FuturePlus Systems Corporation

FS4438 DPv1.2 State Analysis Probe

User Manual

For use with Tektronix Logic Analyzers

Revision – 1.0

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How to reach us *3*

Product Warranty *4*

Limitation of Warranty **4**

Exclusive Remedies 4

Assistance **4**

How to Use This Manual **5**

Introduction *5*

Definitions **5**

Probe Function Overview **6**

FS4438 Input, Output, and Communication, in all modes 6

Aux Port Processing in all modes 6

Hi-speed Link Processing, similar functions in all modes 6

Functions unique to DP1.2 SST mode 6

Functions unique to DP1.2 MST mode 6

Analyzing the DP Bus *7*

Accessories Supplied **7**

Minimum Equipment Required **7**

Probing System Overview *8*

Front Panel **10**

FS4438 Probing Cables **11**

Installing your Software for the First Time **16**

Connecting the Tektronix logic analyzer to the FS4438 ..... **17**

Logic Analyzer System Support files **18**

Offline Analysis **19**

Probe Manager Application **20**

Mode Selection 22

DP 1.1a Mode 22

DP 1.2 Mode SST & MST Probe Manager functions 25

Symbol files **30**

Triggering **31**

The Protocol Disassembler **32**

General Information *43*

Characteristics **43**

Standards Supported 43

Power Requirements 43

Logic Analyzer Required 43

Environmental Temperature 43

Altitude 43

Humidity 43

Testing and Troubleshooting 43

Servicing 43

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Due to the complex nature of the FS4438 and the wide variety of customer target implementations, the FS4438 has a 30 day acceptance period by the customer from the date of receipt. If the customer does not contact FuturePlus Systems within 30 days of the receipt of the product it will be said that the product has been accepted by the customer. If the customer is not satisfied with the FS4438 they may return the FS4438 within 30 days for a refund.

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Introduction

How to Use This Manual

This manual is organized to help you quickly find the information you need.

- **Analyzing the DP Bus** chapter introduces you to the FS4438 and lists the minimum equipment required and accessories supplied for DP bus analysis.
- The **State Analysis** chapter explains how to configure the FS4438 to perform state analysis on your bus.
- The **General Information** chapter provides information on the operating characteristics, and cable header pinout for the FS4438 probe.

Definitions

The following terms are used to describe aspects of the DP bus:

- Lane- One differential signal (2 wires).
- Link - One set of up to 4 DP lanes. The FS4438 handles 1 DP and 1 Aux link.
- SST (Single Stream Traffic), MST (Multi-Stream Traffic)

Probe Function Overview

The FS4438 probe is capable of connecting to DisplayPort links running in any of three modes (v1.1a, v1.2 SST, v1.2 MST) at 3 link speeds (1.62, 2.7 and 5.4 Gbps).

FS4438 Input, Output, and Communication, in all modes

- 8b10b Decode & serial to parallel conversion of serial links: 1, 2, and 4-lane, to 5.4 Gbps.
- Support of two probe cable types (interposer and flying lead).
- No Reference Clock from Target required.
- Serial link input polarity controllable for each lane (lane inversion).
- 8b10b Error Counting indicates signal quality in each lane and is displayed in the log file.
- DDR State processing on 1/10th recovered link clock to logic analyzer.
- 4 Bi-color LED Display, shows status of each lane
- Field upgradeable Flash Memory.

Aux Port Processing in all modes

- Delivery of probed Aux data to Logic Analyzer Pod connectors with single SDR state clock.
- Probing of Hot Plug Detect (HPD) and display status to Logic Analyzer

Hi-speed Link Processing, similar functions in all modes

- Lane Deskew, with ability to tailor the individual DP1.1a, SST and MST deskew functions.
- Training Detect status to Probe Manager and Logic Analyzer Pods (different patterns for DP1.1a & 1.2 Modes).
- Data Descrambling, which may be enabled/disabled.
- Nibble swapping on all secondary packets (excluding unprocessed MST streams).
- Event Decode (different code tables for 1.1a & 1.2 Modes; excluding unprocessed MST streams).
- Pixel Not Recognizer (1 recognizer in DP1.1a or SST Mode, 4 Recognizers in MST Mode)
- Filter (1 Filter in 1.1a or SST Mode, 4 Filters in MST Mode; excluding unprocessed MST streams)
- Error Detection (DP1.1a Mode: 4 sources, 1 LAI bit; DP1.2 Mode: 6 sources, 3 LAI bits)
- Restart Logic allows probe to operate and continue capture through target reboots.

Functions unique to DP1.2 SST mode

- Additional Training Patterns
- Additional Secondary Packets

Functions unique to DP1.2 MST mode

- Control Symbol Descrambling
- Time Slot Counter, 6 bits to Logic Analyzer Pod Connectors
- Processes any set of 4 Virtual Channels, remaining VCs are flagged as “un-processed”
- MST Mode VC Tagging: 4 Selected VCs, with 3-bit tag to Logic Analyzer
- 4 Probe-Stream Processors, to handle any 4 user-selected Streams (Virtual Channels)
    - Event Decode
    - SDP nibble swap
    - Pixel not-recognizer
    - Filter
- MTP Header processing and checking

MST Mode VC Payload Demux and VC Payload Re-mux functions

Analyzing the DP Bus

This chapter introduces you to the FuturePlus Systems FS4438 preprocessor and lists the minimum equipment required for analysis.

The FS4438 is a DP State Analysis preprocessor. The preprocessor can connect to the target by either a cabled interposer, or flying leads. The “sideband” signals, such as AUX and HPD connect to the probe using separate cables. The preprocessor itself is controlled by the Probe Manager software, which runs under Windows and communicates with the preprocessor via a USB cable.

The FS4438 “snoops” a link without significantly degrading its signal integrity. The high speed serial signal is deserialized and processed for packet identification by the FS4438 before being sent to the logic analyzer connections. Additionally, the preprocessor provides trigger and filtering functions. The dis-assembler software running on the logic analyzer provides information regarding the transactions within the captured traffic.

Accessories Supplied

The FS4438 product consists of the following accessories:

- The FS4438 preprocessor, power supply and cable,
- Protocol Disassemblers (FS1194 and AuxPort1_2_Tek), DP v1.2 Probe Manager application and USB driver application on a CD for either Windows XP or 7.
- A USB cable is provided for connecting the FS4438 preprocessor to the Windows machine that the Probe Manager is loaded on.
- 1 DisplayPort cable (2m M-M) to be used between the DP source (or FS1041 interposer) and the DP sink. We STRONGLY recommend the use of this cable as it has been carefully tested to insure it will not disturb signal integrity at HBR2 data rates.
- This User Manual and Quick Start sheet.

Minimum Equipment Required

The minimum equipment required for analysis of a DP consists of the following equipment:

- Tektronix logic analysis frame with logic analysis modules.
- FS1055 cables for connection of the FS4438 to the TLA modules
- A DPI target bus.

Probing System Overview

The architecture of the FS4438 preprocessor and the design of the DP link to be probed should both be thoroughly understood before attempting to use the probe.

The following is a general outline of the steps to be taken when probing a new link. Read the following pages for more specific information.

The FS4438 preprocessor requires the understanding and correct set-up of 4 different systems before a trace should be taken. These systems are

1. Probe Manager software. The software has two installation (.exe) programs associated with it, one to load the USB drivers needed to establish USB connections between the probe HW and the Probe Manager program, and the other is to install the Display Port 1.2 Probe Manager GUI program.

   The USB driver should be installed first.

   All installation programs are located on the CD that comes with the FS4438.

   The USBXpress software is identified as USBXpressInstaller.exe and the Probe Manager software is identified as DisplayPort12_probe_manager_**XXX**.exe, where XXX indicates the PC's OS. The Probe Manager GUI program is supported on the Windows XP or Windows 7 OS and has a separate installation program for each OS. The appropriate installation program must be executed for the OS on which the program will be loaded onto.

   Install SiLabs Driver

   Run the USBXpressInstaller.exe program that is located on the CDROM disk to install the USBXpress driver that provides the USB connection to the probe HW.

   Install Probe Manager Software

   On Windows 7 PCs

   Run the DisplayPort12_probe_manager_7.exe program that is located on the CDROM to install the DP 1.2 Probe Manager GUI software.

   On Windows XP PCs

   Run the DisplayPort12_probe_manager_xp.exe program that is located on the CDROM to install the DP 1.2 Probe Manager GUI software.

   NOTE: The Microsoft .NET Framework must be on the system for the Probe Manager application to load properly.

2. FS4438 probe. This preprocessor requires its own DC power supply which is provided. Additionally, this preprocessor is completely initialized, set-up and controlled by the Probe Manager software that resides on a Windows based system (either stand alone PC or logic analyzer). All communication to the FS4438 preprocessor is by means of the USB port on the PC (or logic analyzer). Improper or incomplete installation of either the correct USB driver or the Probe Manager software will prevent operation of the FS4438.

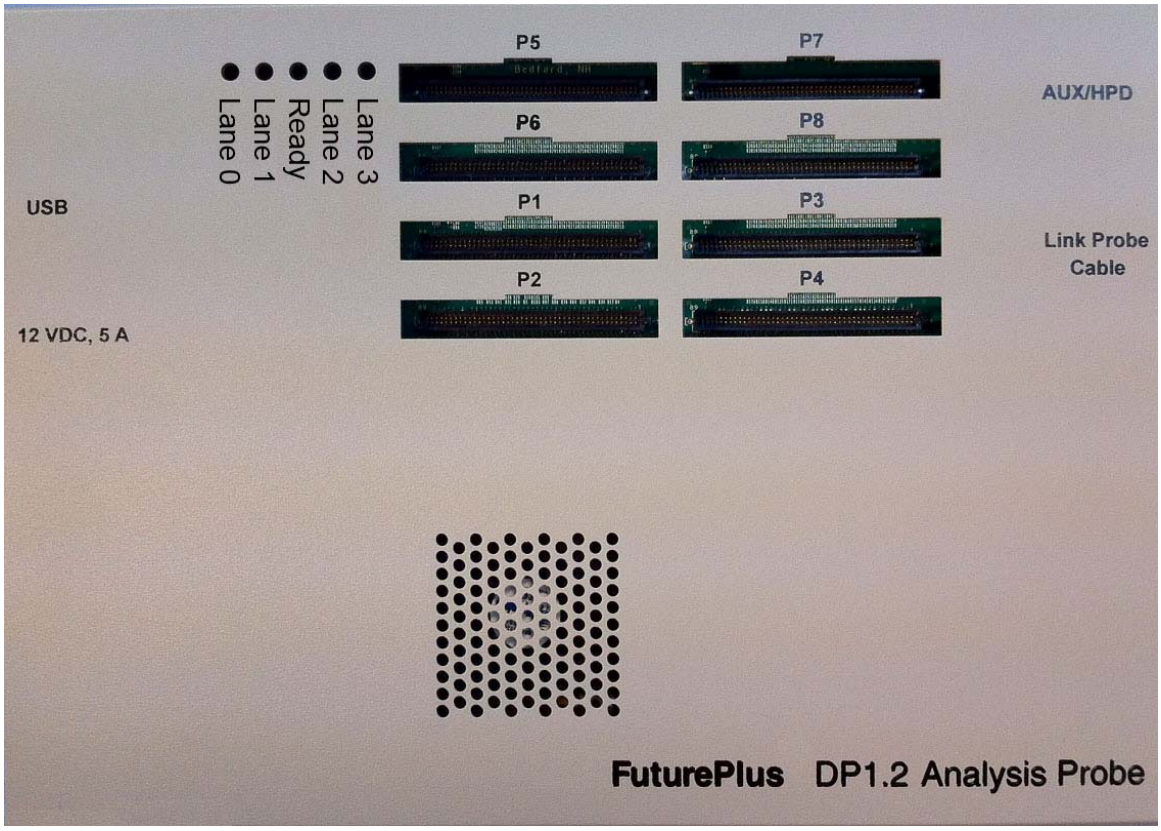
3. Tektronix Logic Analyzer. The System Support files for the logic analyzer are on a CD (FS1194 and AuxPort1_2). Install these files, either for Windows XP or 7, as required and follow the instructions for logic analyzer module (card) interconnections and logic analyzer connections to the FS4438 probe. FS1055 cables are required for connection of the FS4438 to the TLA modules.
4. Target platform. There are several requirements of the DP platform in order to assure that the FS4438 can successfully probe the target's DP link with minimal impact to the link and errors seen at the probe. These requirements are discussed in the Probe Cables section. There are two probing cables, FS1041 interposer or Flying Lead. There are link attributes such as lane inversion, data scrambling, and lane reversal, which need to be defined in the Probe Manager in order for the preprocessor to capture data properly.

It is strongly recommended that the user methodically proceed in the following manner when setting up the probe. There is more detail on each step on page 17.

1. Load the USB driver Installation software into the system that the Probe Manager software will run on.
2. Load the Probe Manager software (USBXpressInstaller.exe) and FS1194/AUX.exe files on the PC and/or logic analyzer.
3. Configure the logic analyzer modules as required, and run the Tektronix Logic analyzer's internal diagnostics. If the analyzer passes, then make the appropriate target probe connections to the FS4438 probe and from the probe to the Tektronix logic analyzer.
4. Connect the appropriate probing cable(s) to the target system, power up the probe. Wait until the "Green" ready light appears on the FS4438. This can take up to 20 seconds after power has been applied to the probe.
5. Open up the Probe Manager application and select the appropriate settings for the probe cable being used and the target link. Check that the expected Pad assignments for the probed link show green. For the first capture turn off all the filters. It is recommended that the first capture be run at HBR rate (2.7Gbps).
6. If the FS4438 preprocessor Lane LEDs are all Green and the first trace file captured on the logic analyzer has no error messages then it is a good indication that all initial settings are correct.
7. A link showing any orange on an LED needs settings for DFEQ, link width, lane reverse or lane inversion adjusted in the Probe Config window.

Depending on the DP target system's data lane signal characteristics, such as jitter tolerance, jitter spectrum and BER, the user may always see some level of orange LED activity and see the corresponding error counts recorded on the analyzer and in the Probe Error Log.

Front Panel



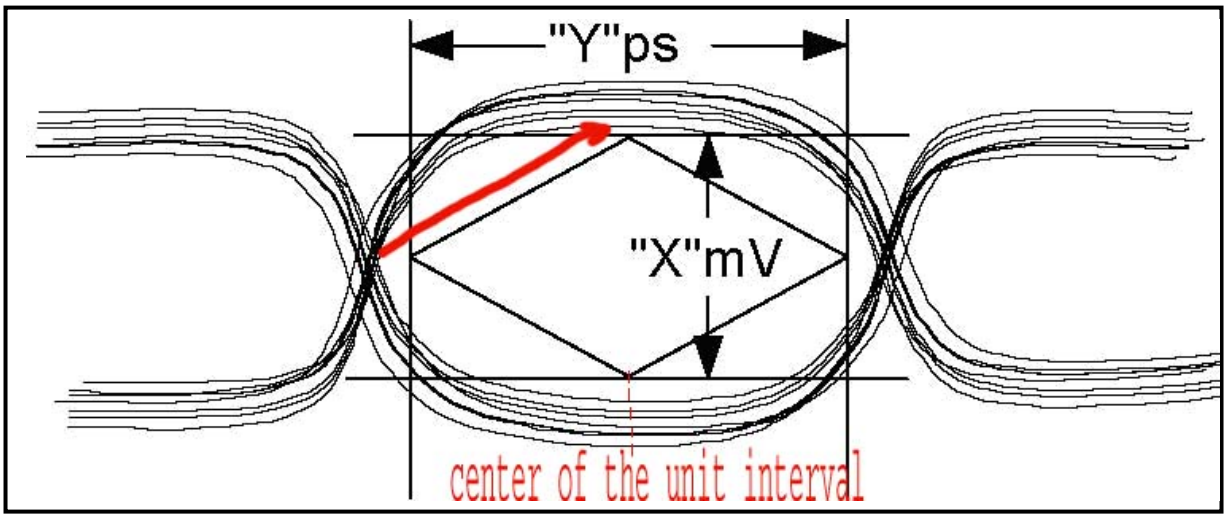
The connections and features of the FS4438 preprocessor include:

- DC input for provided external AC to DC power supply (please note that the use of any other power supply voids the warranty on the FS4438) and USB connections to the Windows PC/169xx analyzer where the Probe Manager software will be loaded.
- Link Probe cable connection for 1 of the probing cables (Interposer or FL)
- Logic Analyzer 90 pin pod connections. P1 – P4 are connections for HS Link, and P5 – P8 are for AUX link. 1 FS1055 cable will connect 2 pods to 1 TLA module connector.
- Cables for connection to AUX and HPD.
- READY LED indicates that the FS4438 Probe firmware is loaded and the probe is ready to capture DP traffic.
- LED indication of Lane status.

Lane Status LED color	Meaning
Green	Lane OK
Dark	Lane not active, or Probe stopped
Orange	Data Invalid (8b10b error)
Red	RX Error (loss of sync or PLL lock)

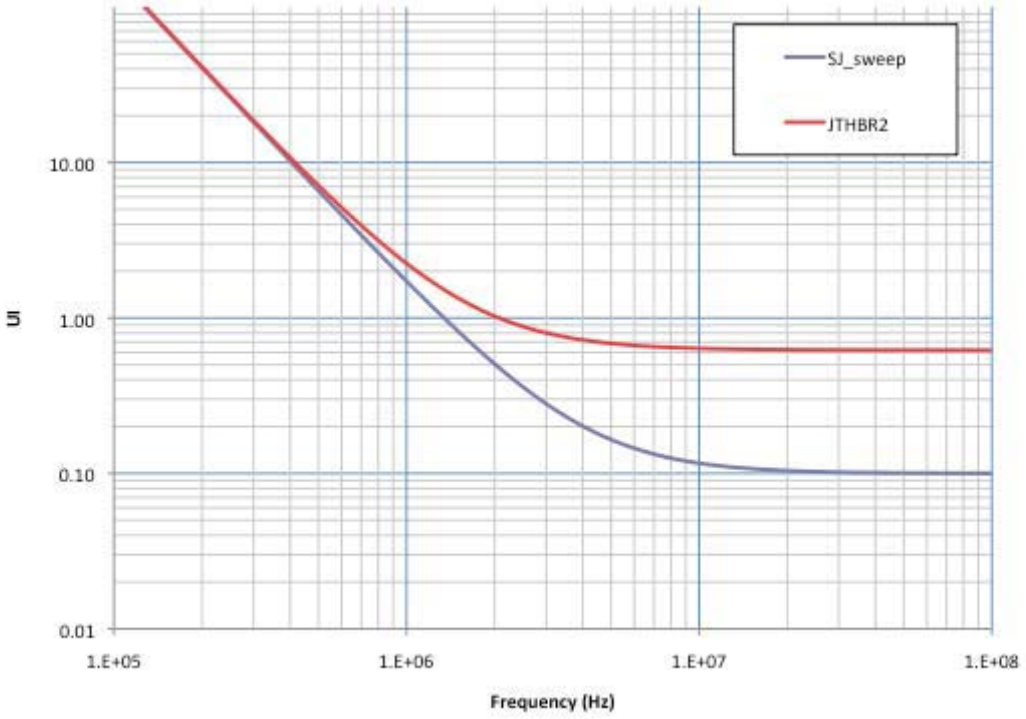
Target DP Link requirements

The eye requirements are measured by eye height and eye width, forming a diamond shape. These requirements are listed below and described pictorially. The shape of the eye as seen by the FS4438 must closely resemble the wave shape shown below. **Specifically the eye opening must not show a decrease in amplitude prior to reaching the center of the unit interval.**



Description	Specification for 2.7Gbps	Specification for 5.4Gbps
Min Eye height at footprint pad [1]	175mV Vdiff p-p	90mV Vdiff p-p
Min Eye Width at probe point	.45 UI (Jitter tolerance of 0.55UI)[3]	.45 UI (Jitter tolerance of 0.55UI)[3]
Length Matching Requirements- Differential Pair	+/-5mil [2]	+/-5mil [2]
Skew tolerated between lanes of a link	24 ns	24 ns

In order for the FS4438 to achieve a low error rate for the acquired data on the DisplayPort Main Link, the Jitter Spectrum for the target must be within the jitter tolerance shown below. **Users not adhering to this specification do so with the knowledge that errors may be seen on the FS4438 and incorrect protocol decode could result.**



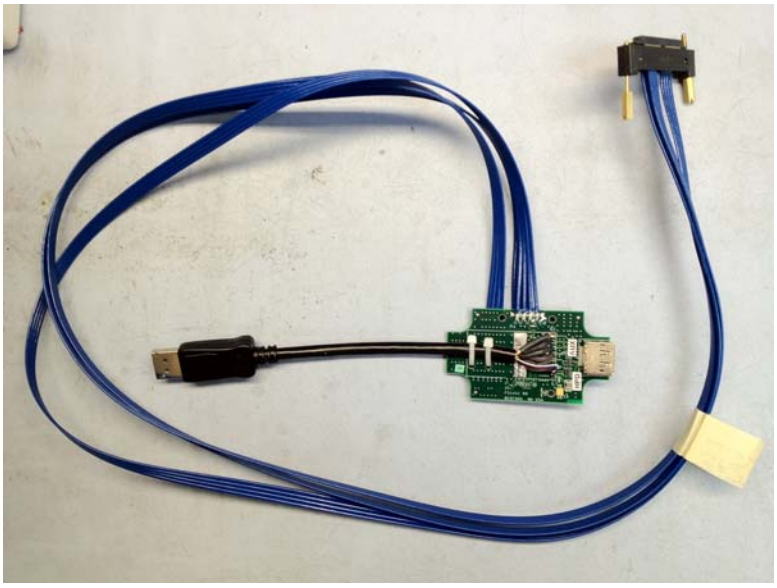
The FS4438 can be configured with different probing cables dependent on what the user requires:

FS1041	DisplayPort Interposer
FS1036B	Flying lead probing cable for x1 to x4 link

FS1041 DP Interposer cable

The FS1041 is a DisplayPort cable interposer that allows for probing of the DisplayPort bus between the motherboard (Source) and the monitor (Sink). One end of the interposer has a short cable with a DisplayPort connector that will mate with the motherboard. The other end of the FS1041 will have a DisplayPort connector that mates with the source device (monitor). The body of the FS1041 is a board assembly that allows the probing of the high speed Main Link, Aux Channel and HPD. Aux Channel and HPD have the 3 pin header stake pins described in this document, which will mate with the two cables from the FS4438. The high speed Main Link will be tapped and go to a soldered on cable. The other end of the cable will go to the FS4438 instrument end header.

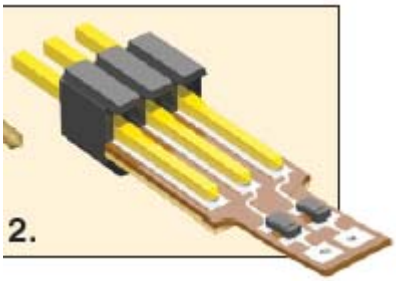
The probe cable should be attached to the FS4438 and carefully secured with the 2 captive fasteners on the cable.

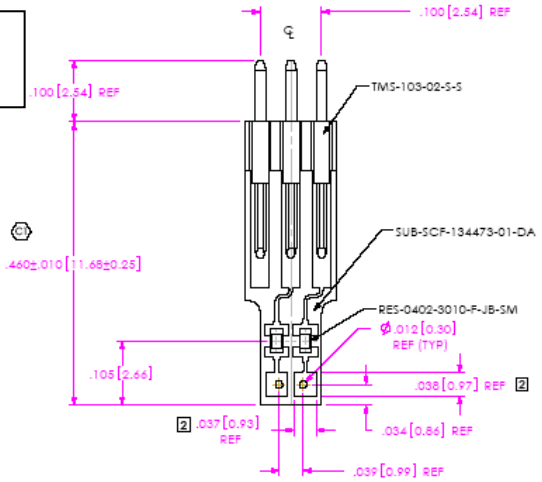


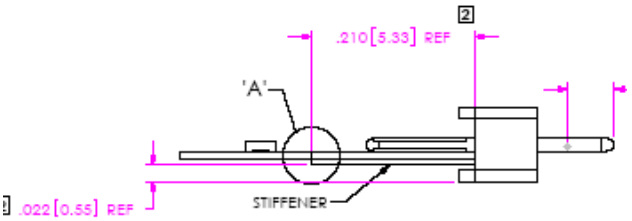
Flying Lead Probing (FS1036B cable assembly)

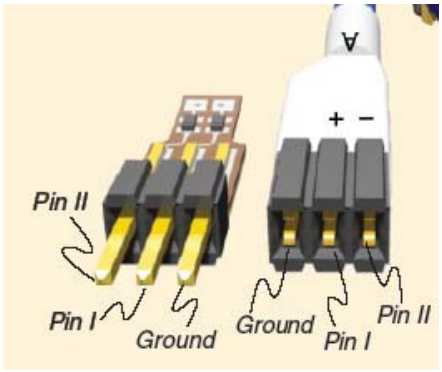
The FuturePlus FS1036B high speed flying lead probe can be connected anywhere on the target that the user thinks an adequate eye can be obtained. The FS1036B was designed to be used right at the AC coupling capacitors incorporated into the DisplayPort Main Link traces. The FS1036B flying lead cable assembly allows the FS4438 preprocessor to connect to components on the target board by means of directly soldering a flex pcb to a component or feature on the target pcb, then connecting the header on the flying lead cable to the other end of the flex pcb.

FS1036B is for use on the Main Link not the Aux Channel or Hot Plug Detect signals





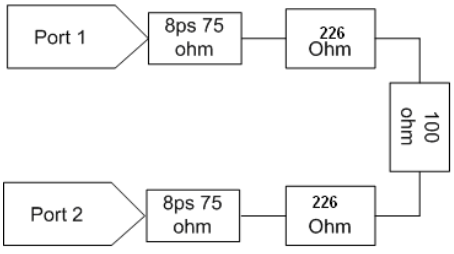




A few general guidelines about the use of the flying lead cable

1. There is an instruction booklet with the FS1036B cable that provides detail on how to solder the flex pcb to your board. Refer to this document.
2. Polarity matters. Makes sure you know how the + and – sides of the signal are connected. Reversal of polarity can be performed in the Probe manager Configuration screen.
3. The ground of the FS1036B is not connected to the target but to the shield of the cable and to the ground of the Preprocessor

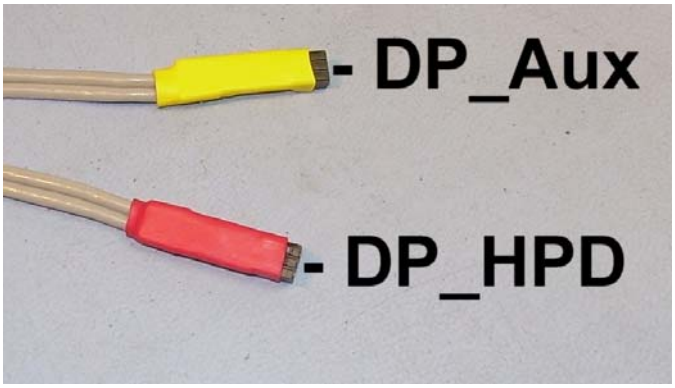
Users should simulate their system to ensure that the FS1036 will not interfere with the target and the appropriate eye will be presented at the probe tip. The model below can be used for this simulation



AUX and Hot Plug Detect (HPD) signals

The AUX and HPD signals for DP need to be connected to the FS4438 preprocessor separately from the data link probing cables. There are uniquely identified and labeled cables for doing this. **These must be properly oriented for polarity.**

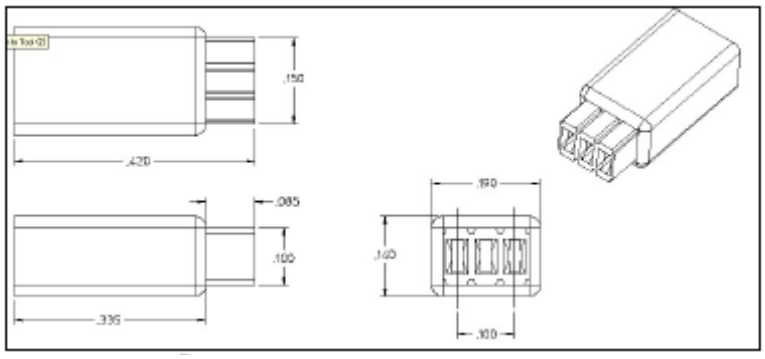
The DP AUX channel requires a high speed differential connection using a Samtec .050 header where pins 1 and 3 are AUXp and AUXn. The HPD signal has its own cable that also connects to a .050 header, pin 1 is the signal and pin 2 is the ground connection.



NOTE: These signals cannot see voltages higher than 4 VDC or there is a risk of damaging the preprocessor.

The KOV for these cable headers is shown below. The mating 3 pin header is part number:

Through-hole: Samtec TMS-103-02-S-S, Surface mount: Samtec FTR-103-02-S-S .



DisplayPort Auxiliary Channel – MUST be plugged in correct orientation

Pin 1	Pin 2	Pin 3
DP_AUX_P	NC	DP_AUX_N

DisplayPort Hot Plug Detect

Pin 1	Pin 2	Pin 3
DP_HPD	GND	NC

Installing your Software for the First Time

The following outlines the software installation procedure when using the preprocessor for the first time. Please do not attach the preprocessor to the analyzer or computer that will be controlling the preprocessor until told to do so.

1. Place the software CD that came with the product into the logic analyzer or computer that you will be installing the software on. In the case of a machine that does not have a CD drive, the machine will either have to be put on a network and the files loaded remotely or the CD files can be transferred from a USB drive.
2. Navigate to the installation CD using Windows explorer and install the following files in this order.
    a. Silabs USB driver installation software folder - USBXpressInstaller.exe
    b. DisplayPort12_probe_manager_7.exe. (Win7 version vs XP version)
    c. FS1194 and AuxPort1_2_Tek.exe Protocol Dis-assemblers (Win7 version vs XP version)
3. Once all the above files have been installed, connect the FS4438 to the analyzer/computer via the USB port. Power on the FS4438 probe.

Once all the previous steps have completed all necessary software as well as USB drivers will be installed. This procedure only needs to be done on initial install. You may now go to the desktop and click on the “DisplayPort 1.2” icon to start the probe manager.

*If you are installing on a PC to only control the FS4438 then you can omit the installation of the FS1194 and AUX.exe, but you must follow the rest of the steps.

For instructions on loading system files please refer to the section on loading system files later in this manual.

Connecting the Tektronix logic analyzer to the FS4438

The FuturePlus Systems FS4438 connectors are designed to use FS1055 cables to connect to the module connectors on the appropriate Tektronix logic analyzer cards as shown below:

	DP 1.2 Main Link X1, X2, X4 <=2.7 GB/s (FS4438)	DP 1.2 Main Link X1, X2, X4 5.4 GB/s (FS4438)	DP 1.2 Aux Channel (FS4438)
Max LA Input Frequency	270 MHz	540 MHz	67 KHz
Channels Required	68	68	68
TLA7AAx, TLA7ACx	1 TLA7AA4	Not Supported	1 ea TLA7AA3 or 1 ea TLA7AA4, 235 MHz 1 ea TLA7AC3 or 1 ea TLA7AC4, 235 MHz
TLA7BBx	1 ea TLA7BB3 or TLA7BB4, 750 MHz for 1.62 Gb/s or 2.7 Gb/s	1 ea TLA7BB3 or TLA7BB4, 750 MHz for 1.62 Gb/s or 2.7 Gb/s	1 ea TLA7BB3 or 1 ea TLA7BB4, 750 MHz
TLA7NAx	Not Supported	Not Supported	

Logic Analyzer		FS4438	Comment
High Speed			
Card 1 Pod	A3,A2	P1	Clock
	D3,D2	P2	
	A1,A0	P3	
	D1,D0	P4	
AUX			
Card 2 Pod	A3,A2	P5	Clock
	D3,D2	P6	
	A1,A0	P7	
	D1,D0	P8	

When probing a single direction of an x1, x2 or x4 link, the FS4438 drives 4 pods of signals to the logic analyzer.

It is important that before you load a system file you initiate a self-test on all your modules installed in your logic analyzer to insure all modules are working properly.

Logic Analyzer System Support files

From the system window of the TLA application, select a logic analyzer module. After selecting the module in the System window, either right click the mouse and select “Load Support Package” or go to File->Load Support Package. After clicking “Load Support Package” a list of installed support packages will appear. Select the support package that matches the desired analysis requirements. The dis-assembler will load along with the system file. If you are analyzing more than 1 link, simply choose another analyzer module from the system window and select “Load Support Package” to load the second module.

The analyzers supported by the FS4438 system files are theTLA7AA4 cards and TLA7BB cards

DP – x1, x2, x4 DP link analysis. Requires 2 FS1055 cables and 68 logic analysis channels.

AUX – AUX analysis. Requires 2 FS1055 cables and 68 logic analysis channels.

Offline Analysis

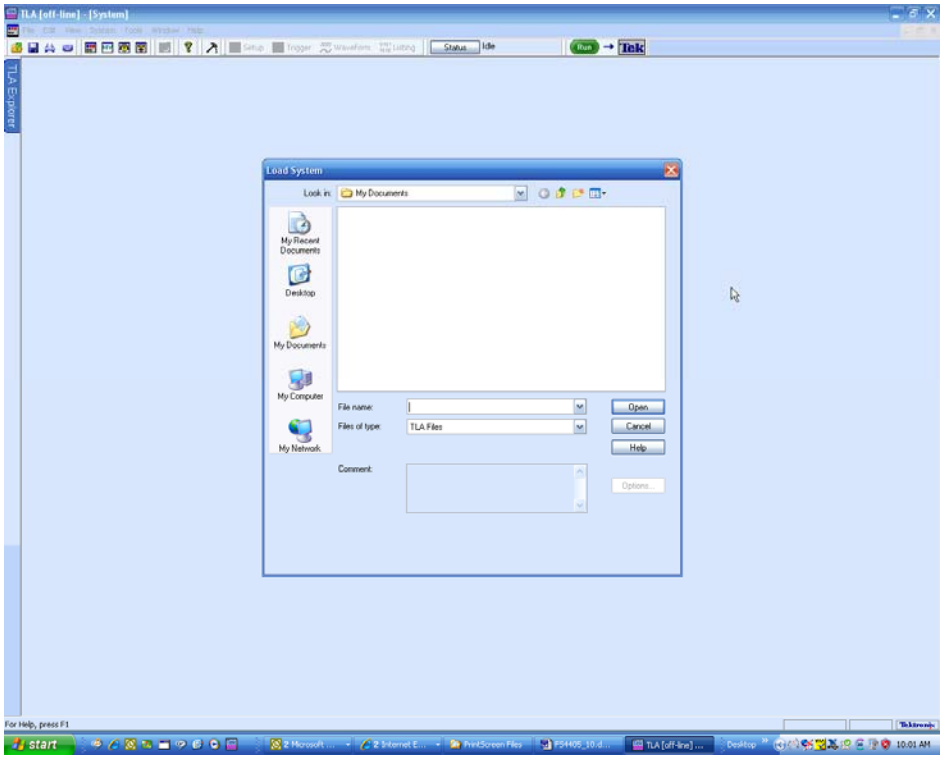
Data that is saved as a *.tla file, can be imported into the TLA7xxx environment for analysis. You can do offline analysis on a PC if you have the TLA7xxx operating system installed on the PC, if you need this software please contact Tektronix.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

In order to view decoded data offline, after installing the TLA7xxx environment on a PC, you must install the FuturePlus software. Please follow the installation instructions for “Setting up TLA7xxx analyzer”. Once the FuturePlus software has been installed follow these steps to import the data and view it.

From the desktop, double click on the Tektronix TLA icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select Cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

Open the .tla file using the File, Load System menu selection and browse to the desired .tla file.



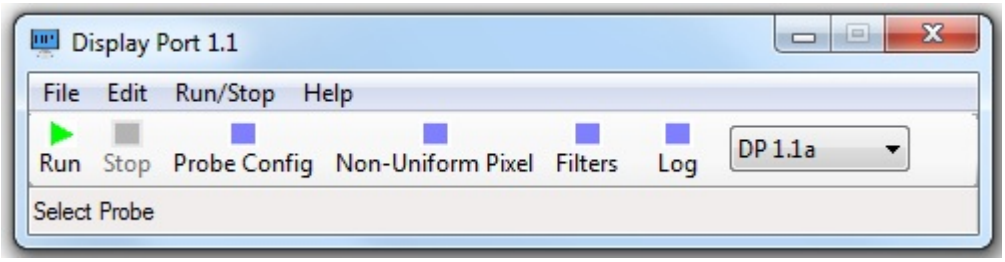
Probe Manager Application

The USBXpress drivers must be installed before the probe manager GUI program can be installed. The drivers can be installed by running the USBXpressInstaller.exe program that is located on the CD provided in the Documentation packet.

The USBXpress drivers installation software can be found as the USBXpressInstaller.exe file on the CD provided in the Documentation package. Insert the CD into the computer that will be used to control the FS4438 probe. This computer must have a USB connection. Using Windows File Manager, Run the USBXpressInstaller.exe (by double clicking it) and following the subsequent directions that follow.

Similarly, the DisplayPort12_probe_manager_7.exe (if you are running Windows XP then select the DisplayPort12_probe_manager_XP.exe file) can be installed by double-clicking the appropriate program on the CD, which initiates the installation software on the computer and places an icon on the desktop. Follow the directions that follow including agreeing to the license terms, once the software installation is complete click on finish. To start the program manager simply double click its desktop icon.

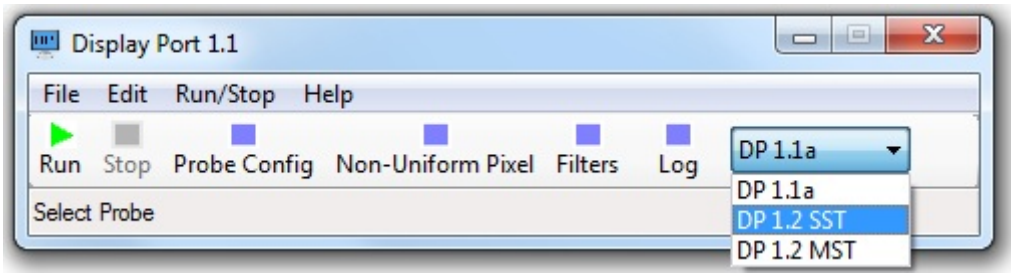
The Probe Manager application detects all FS4438 probes that are connected to the USB bus and allows the user to select which preprocessor will be controlled by the current instance of the Probe Manager application from the initial screen as seen below.



The user configures and controls the preprocessor from the main form, which is composed of a menu bar, a tool bar and a status message bar. The menu bar provides options that allow the user to configure and run the probe. The tool bar provides options to configure the preprocessor and the status bar displays the probes current status and/or any errors that may have been encountered. Error messages displayed in the status bar are also logged in the Log Form if logging is enabled.

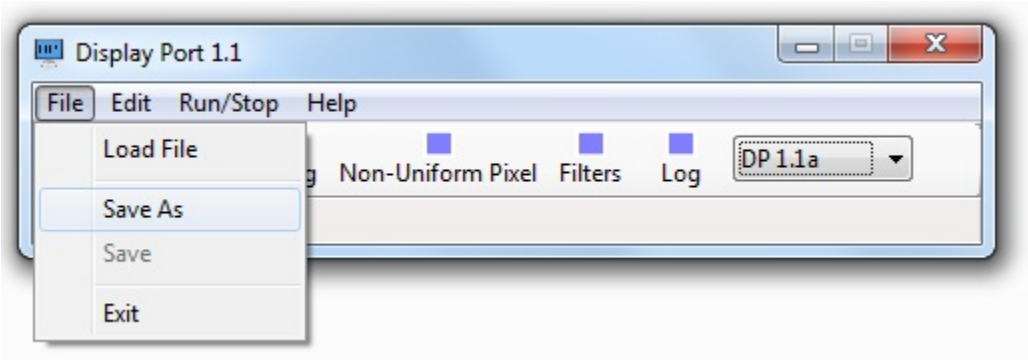
The “mode selection” drop down box gives the user the choice of one of three modes to choose for the probe to run in.

- DP version 1.1a protocol at either 1.67 or 2.7Gbps link rate
- DP version 1.2 Single Stream (SST) at either 1.67, 2.7 or 5.4 Gbps.
- DP version 1.2 Multi Stream (MST) at either 1.67, 2.7 or 5.4 Gbps.



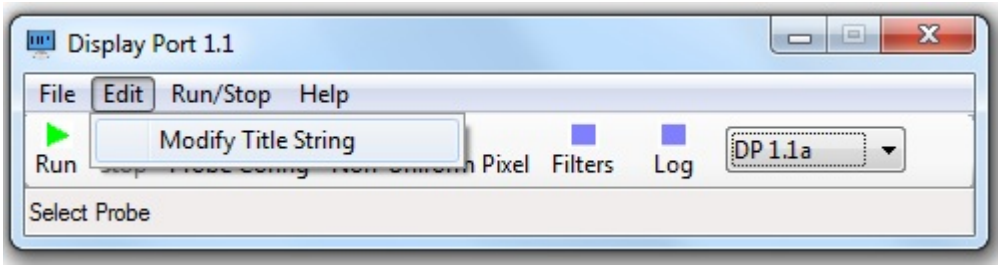
The menu bar contains the following options:

File



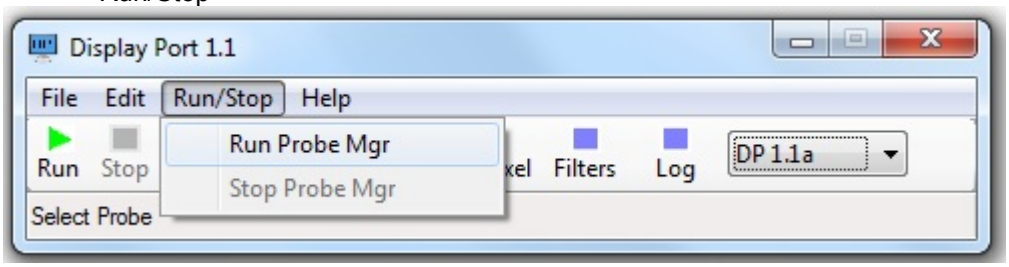
- Load File – Displays an open file dialog in which the user may navigate to and open the file contains a previous session's saved probed settings.
- Save As - Displays a save file dialog in which the user may specify where a preprocessor settings system file may be saved.
- Exit – Shut down the application.

Edit



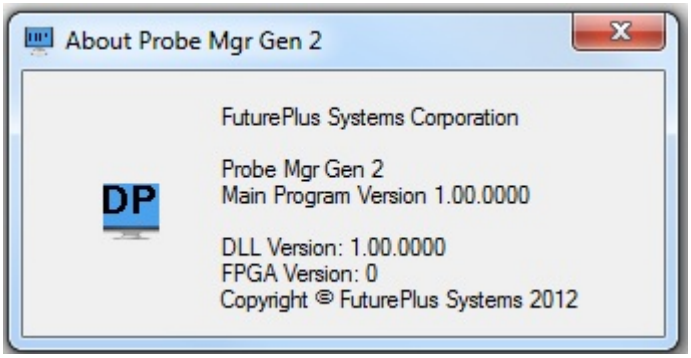
- Modify Title String – Allows the user to specify the title string that appears in all sub-dialog's title bar. This is helpful when running multiple probes.

Run/Stop



- Run Probe Mgr – Running the preprocessor with the current settings. This is an alternative to clicking the tool bar Run button.
- Stop Probe Mgr - Stop the probe. This is an alternative to clicking the tool bar Stop button.

Help



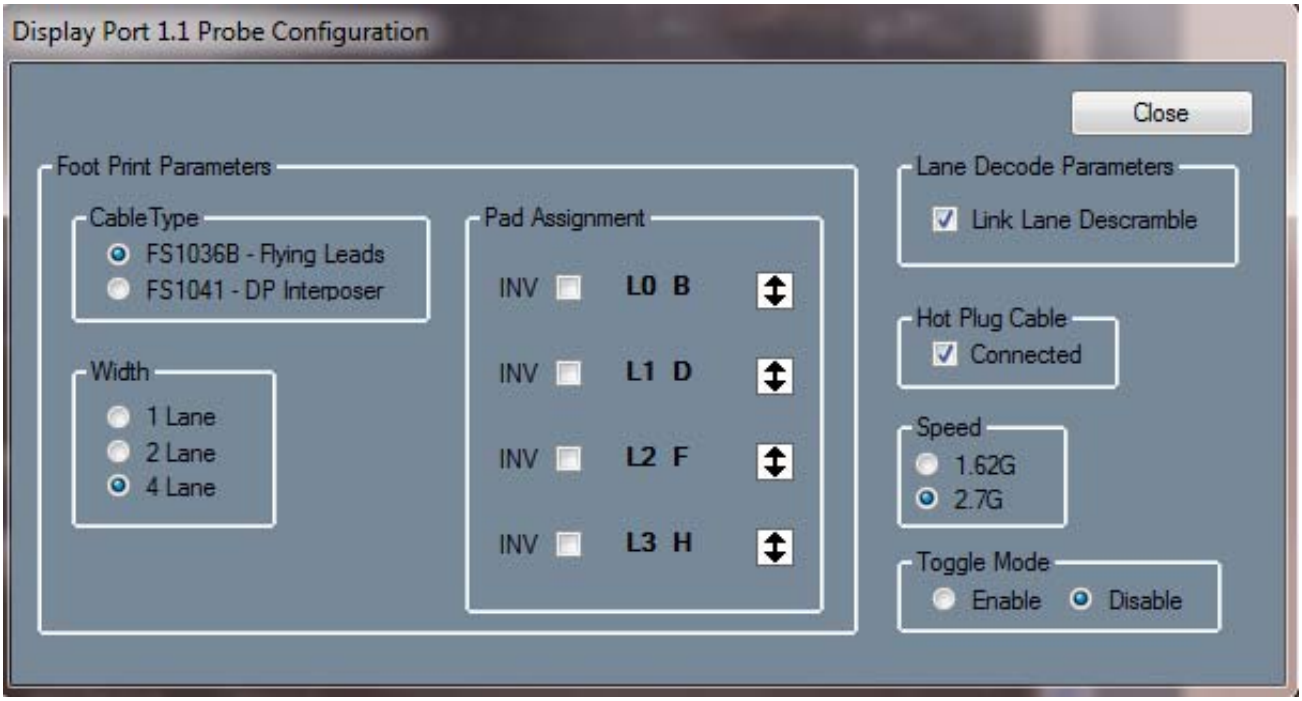
- About – Displays version numbers for the Probe Manager application and FPGA configuration.

Mode Selection

The Probe Manager application provides different selections to the user based on the "Mode" that the FS4438 Probe is set to run in. The sections of this User Manual that describe the configuration and use of the Probe Manager are organized by Mode.

DP 1.1a Mode

Operation of the FS4438 in this mode will match the VESA Protocol specs for v1.1a on links of x1, x2, or x4 at either 1.62 or 2.7 Gbps. The Configuration selections are shown below:

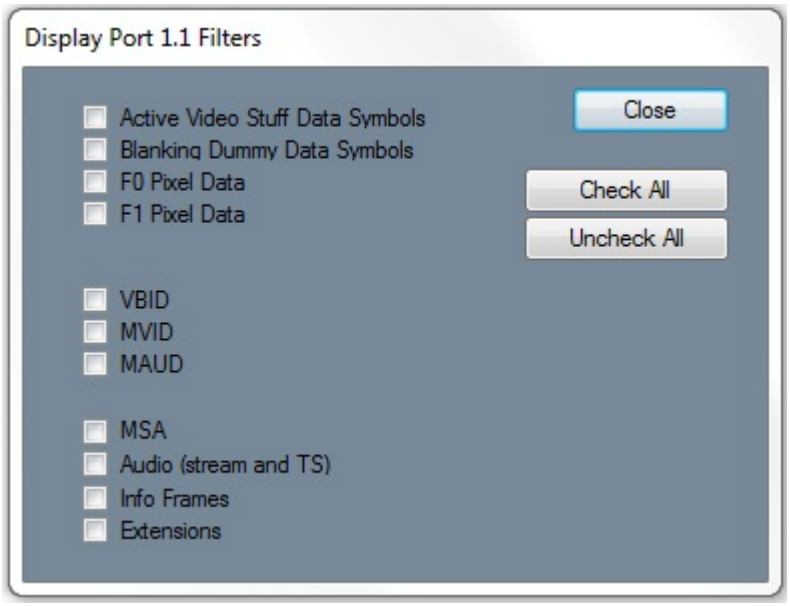


Note: there is no Config required for Aux signals

The functions provided on this screen include:

- Selection of the Probing Cable type and Lane Width
- Lane Inversion can be selected on an individual channel basis by clicking the INV button associated with each lane.
- While the preprocessor is stopped, signal activity indicators are provided on each channel. Signal presence is indicated by an up-down arrow symbol and a lack of signal presence is indicated by a flat horizontal line symbol. When the probe is in Run mode, signal activity is indicated by green or red (no activity).
- Selection of Lane Reversal on each link.
- Link Lane Descramble On or Off
- Hot Plug Cable (HPD) Connection – If Connected is selected, then Aux decode requires the HPD signal for operation.
- Selection of Link rate, either 1.62 or 2.7 Gbps.
- Selection of Toggle mode. When activated, the preprocessor output signals to the logic analyzer pods and the link status LEDs are toggled.

Mode 1.1a Filter - a comprehensive suite of predefined filter functions to apply to the high speed Link. These filters are state based, which means that the event has to occur on all active lanes for it to be filtered.

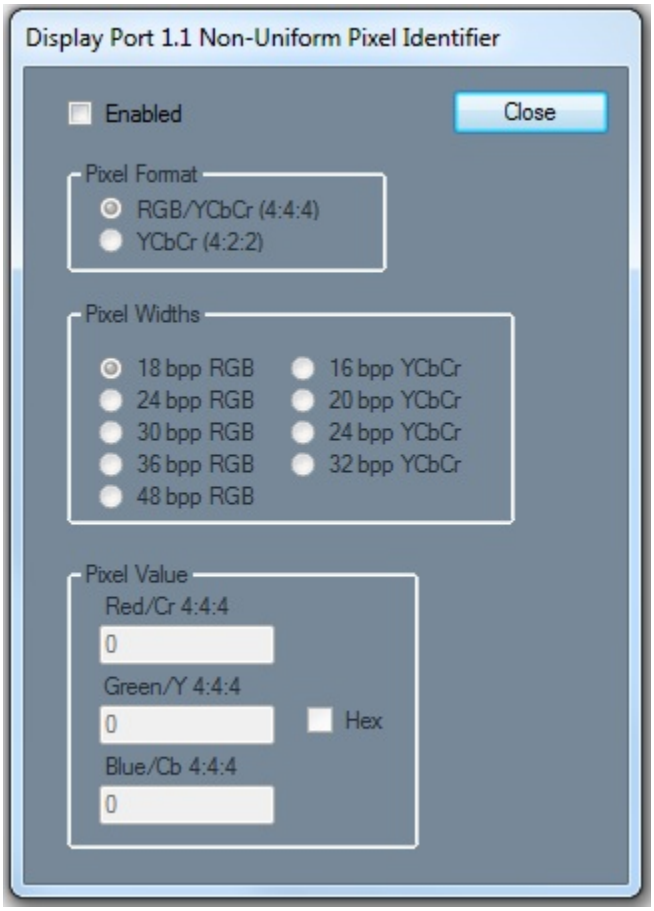


Filtering out unwanted traffic such as dummy data symbols can extend the storage capabilities of the logic analyzer. Filtering out irrelevant bus traffic can help users focus on specific packets of interest.

To filter out any particular traffic type, click on the appropriate box so a √ appears and click apply. You must restart the preprocessor by pressing the green Run button so the new values will be written to the preprocessor hardware.

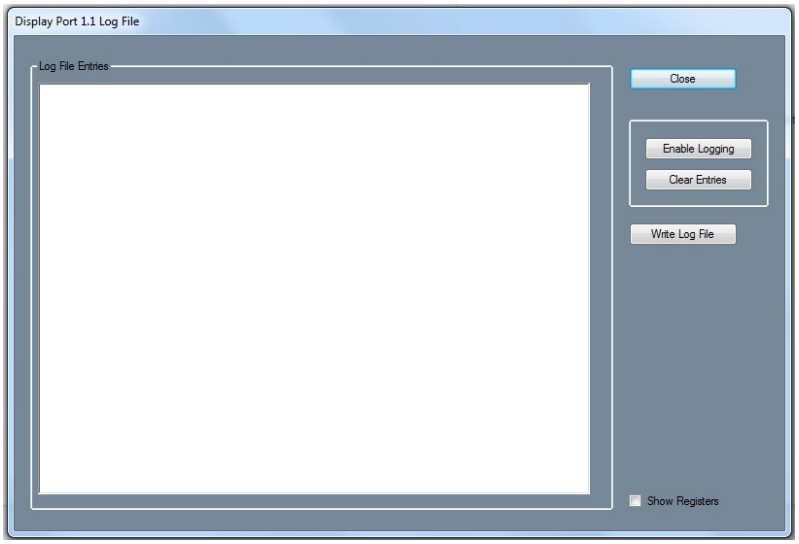
When "Decode Pixel States" is selected in the Protocol Decoder Preferences, then you cannot filter Control Symbols.

Non-Uniform Pixel Identifier – The purpose of this tool is that it is to be used when the pixel values are all expected to be a single value, which the user sets in the form shown below. The FS4438 will produce a Trigger if it sees any Pixel value that is **NOT Equal** to the set value.



Log File - Once started, logging continues even if the preprocessor is stopped and started, or if the log window is closed and re-opened. The log file will not repeat an error that repeats itself constantly.

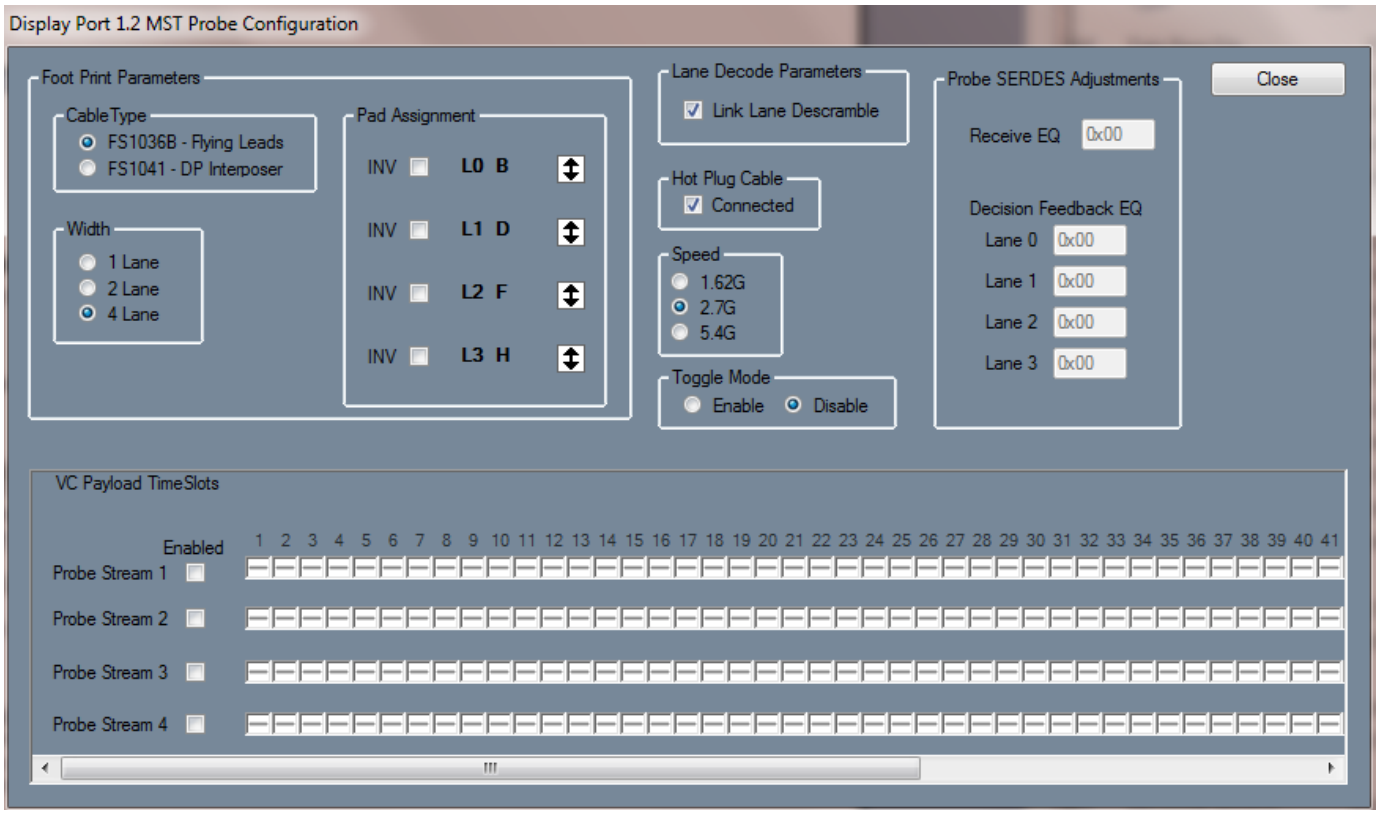
Once a preprocessor has been stopped, the log entries can be written to a file of the user's choice by clicking the Write Log File button.



DP 1.2 Mode SST & MST Probe Manager functions

There are several changes to the Probe Manager Screens when DPv1.2 mode is selected.

The Probe Configuration screen has the following changes.



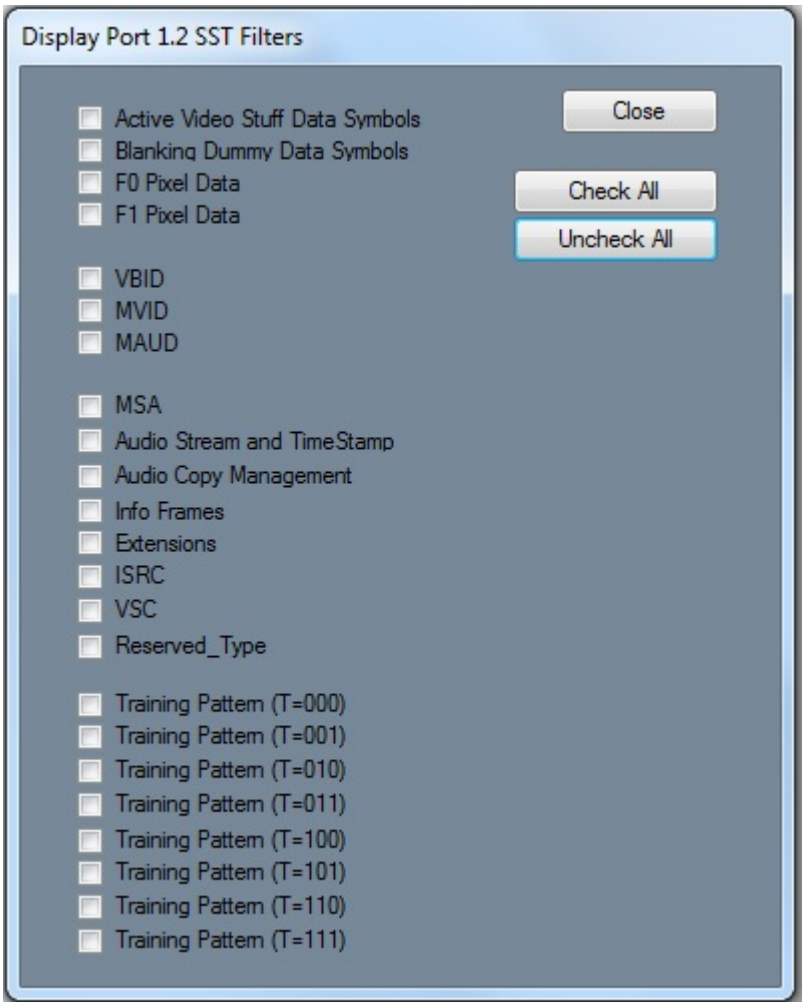
Probe SERDES adjustments - are used to "tune out" Receive errors shown as Orange LEDs on the front panel of the FS4438. These adjustments are for use at HBR2 only. The DFEQ setting may provide the most effect. If the default settings do not work, we would recommend adjusting DFE up to about 0A as a stating point.

- Receive EQ – is set at 2 (hex), the range for the setting is from 0 – 7.
- DFEQ is set at 07 (hex), the range of values 0 – 1F. This adjustable on a per lane basis to allow for SI variation between lanes.

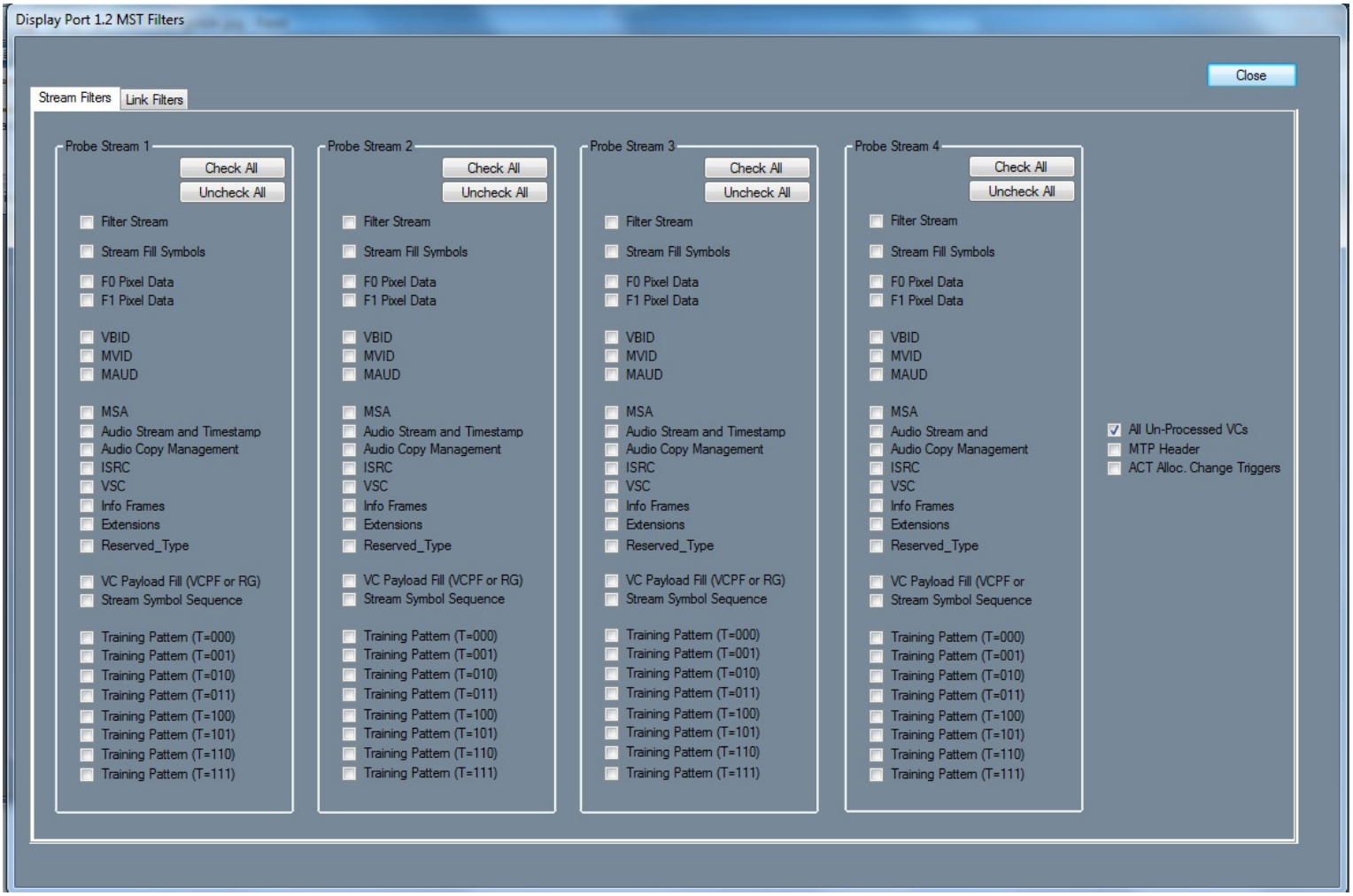
VC (Virtual Channel) Payload Time slots – In MST mode only, the v1.2 spec allows for video display information to be broken up into 64 Payload Time Slots that are assigned to the individual video streams (VCs) that are being carried on the DP link. This dialog allows the user to assign each possible Time Slot to any of the up to 4 video streams that the FS4438 probe will capture and decode.

The information relating the VCs to each Time slot can be determined from the AUX channel State listing for registers at addresses # 001C00:2h and 002C00:FFh.

The Filter Function has the following changes for v1.2 SST mode based on additional secondary data packet types and Training patterns that were added to the DP specification:



The Filter Function has the following changes for v1.2 MST, which extends the SST Filtering functions to include a separate Filter function for each Stream defined in the Configuration form and adds the ability to filter within each stream based on it's VC Payload fill or Stream Symbol.



State Analysis

This chapter explains how to use the FS4438 to perform State Analysis.

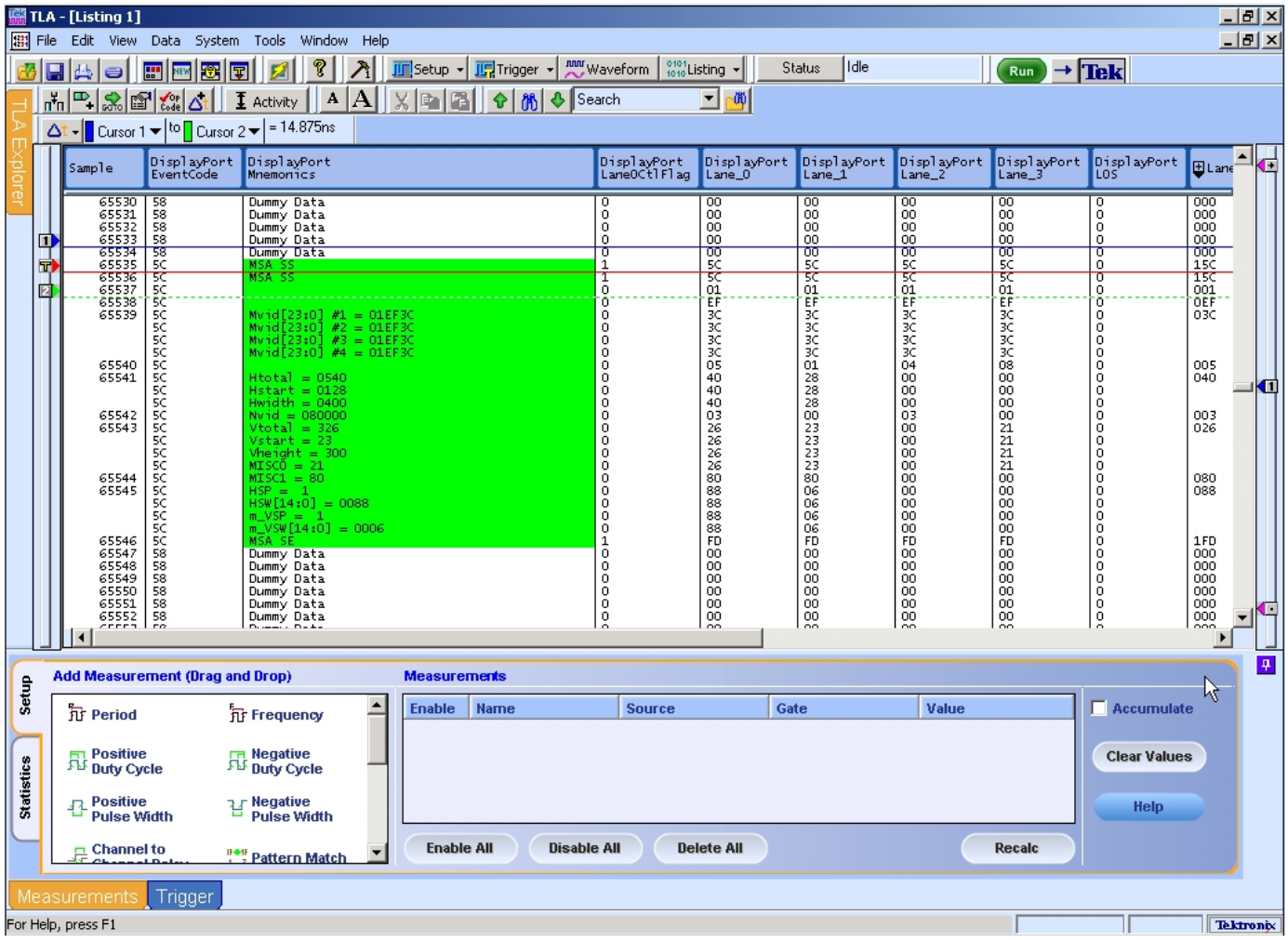
From the system window of the TLA application, select a logic analyzer module. After selecting the module in the System window, either right click the mouse and select “Load Support Package” or go File->Load Support Package. After clicking “Load Support Package” a list of installed support packages will appear. Select the support package that matches the desired analysis requirements. The dis-assembler will load along with the system file. If you are analyzing more than 1 link, simply choose another analyzer module from the system window and select “Load Support Package” to load the second module.

A list of Support Packages are as follows:

FS1194: DisplayPort

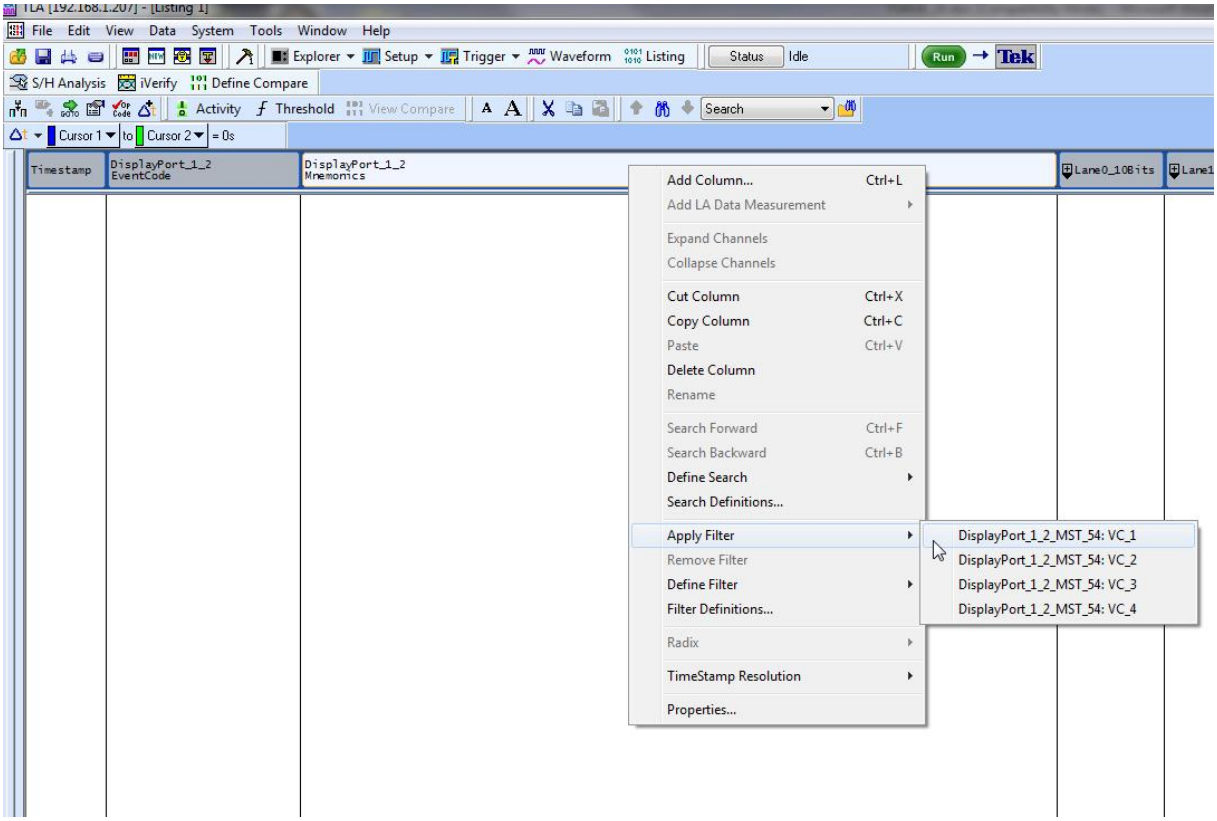
AuxPort: DisplayPort Auxiliary Port

The following is an example listing screen showing the protocol decode provided by the Disassembler for DisplayPort



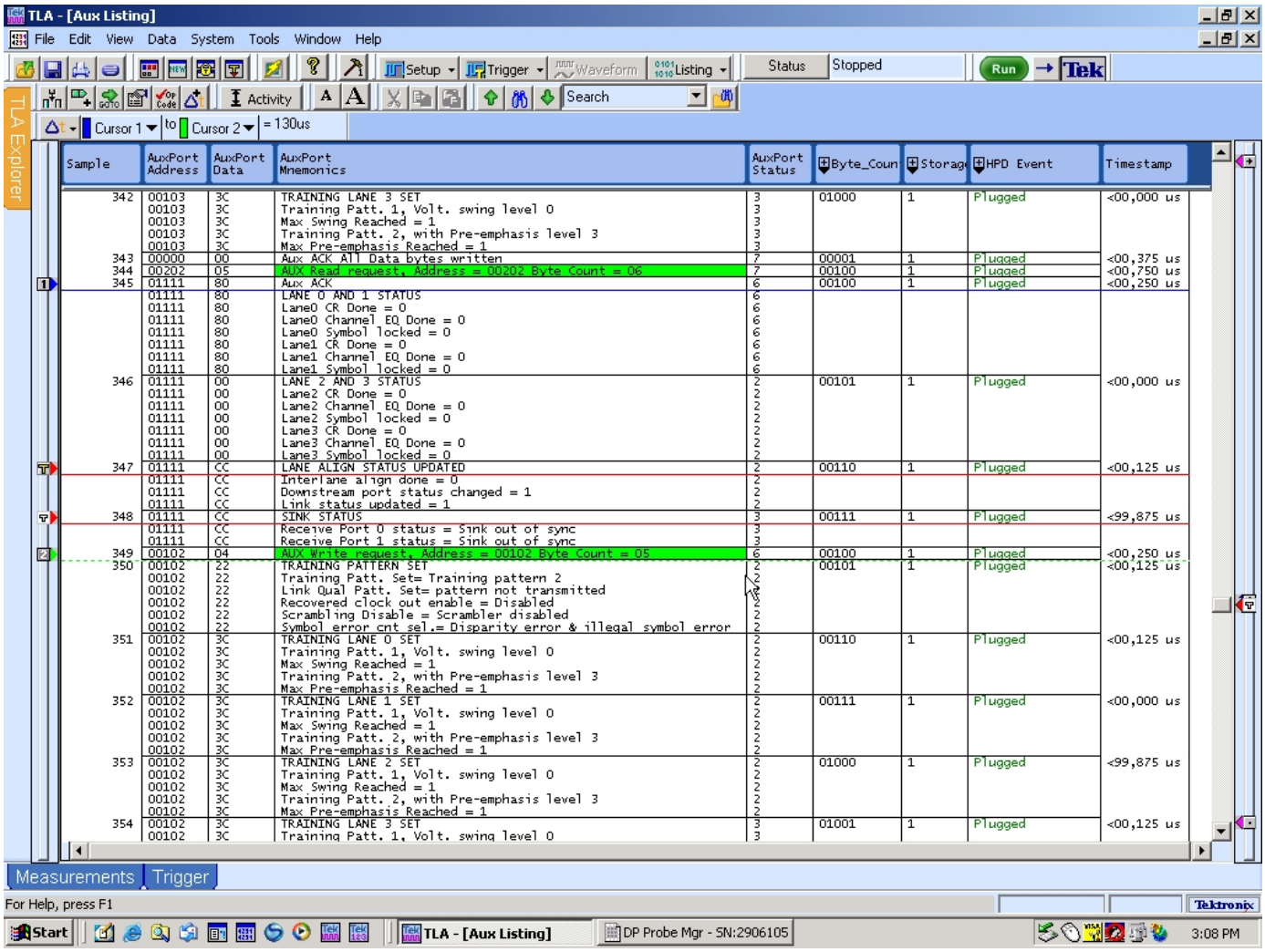
Viewing MST in listing window

In order to provide an uncluttered display of each virtual channel it is best to enable a filter in the listing window to show only the virtual channel the user is interested in. Each of the support packages for MST has pre-defined filters that can easily be enabled.



To enable a filter right click on any column of the listing window, on the pop up window select “Apply Filter” then select any of the 4 filters that appear to the right. When VC_1 is chosen the only data that will be shown in the listing window will be data from virtual channel 1. The user can add 3 more listings and apply the appropriate filter to each listing to view all 4 virtual channels in their own listing window.

The following is an example listing screen showing the protocol decode provided by the Disassembler for AuxPort.


TLA - [Aux Listing]
File Edit View Data System Tools Window Help
Setup Trigger Waveform Listing Status Stopped Run Tek
Activity Search
Cursor 1 to Cursor 2 = 130us
TLA Explorer
Sample | AuxPort Address | AuxPort Data | AuxPort Mnemonics | AuxPort Status | Byte_Coun | Storage | HPD Event | Timestamp
342 00103 3C TRAINING LANE 3 SET 3 01000 1 Plugged <00,000 us
00103 3C Training Patt. 1, Volt. swing level 0 3
00103 3C Max Swing Reached = 1 3
00103 3C Training Patt. 2, with Pre-emphasis level 3 3
00103 3C Max Pre-emphasis Reached = 1 3
343 00000 00 Aux ACK All Data bytes written 7 00001 1 Plugged <00,375 us
344 00202 05 AUX Read request, Address = 00202 Byte Count = 06 7 00100 1 Plugged <00,750 us
345 01111 80 Aux ACK 6 00100 1 Plugged <00,250 us
01111 80 LANE 0 AND 1 STATUS 6
01111 80 Lane0 CR Done = 0 6
01111 80 Lane0 Channel EQ Done = 0 6
01111 80 Lane0 Symbol locked = 0 6
01111 80 Lane1 CR Done = 0 6
01111 80 Lane1 Channel EQ Done = 0 6
01111 80 Lane1 Symbol locked = 0 6
346 01111 00 LANE 2 AND 3 STATUS 2 00101 1 Plugged <00,000 us
01111 00 Lane2 CR Done = 0 2
01111 00 Lane2 Channel EQ Done = 0 2
01111 00 Lane2 Symbol locked = 0 2
01111 00 Lane3 CR Done = 0 2
01111 00 Lane3 Channel EQ Done = 0 2
01111 00 Lane3 Symbol locked = 0 2
347 01111 CC LANE ALIGN STATUS UPDATED 2 00110 1 Plugged <00,125 us
01111 CC Interlane align done = 0 2
01111 CC Downstream port status changed = 1 2
01111 CC Link status updated = 1 2
348 01111 CC SINK STATUS 3 00111 1 Plugged <99,875 us
01111 CC Receive Port 0 status = Sink out of sync 3
01111 CC Receive Port 1 status = Sink out of sync 3
349 00102 04 AUX Write request, Address = 00102 Byte Count = 05 6 00100 1 Plugged <00,250 us
350 00102 22 TRAINING PATTERN SET 2 00101 1 Plugged <00,125 us
00102 22 Training Patt. Set= Training pattern 2 2
00102 22 Link Qual Patt. Set= pattern not transmitted 2
00102 22 Recovered clock out enable = Disabled 2
00102 22 Scrambling Disable = Scrambler disabled 2
00102 22 Symbol error cnt sel.= Disparity error & illegal symbol error 2
351 00102 3C TRAINING LANE 0 SET 2 00110 1 Plugged <00,125 us
00102 3C Training Patt. 1, Volt. swing level 0 2
00102 3C Max Swing Reached = 1 2
00102 3C Training Patt. 2, with Pre-emphasis level 3 2
00102 3C Max Pre-emphasis Reached = 1 2
352 00102 3C TRAINING LANE 1 SET 2 00111 1 Plugged <00,000 us
00102 3C Training Patt. 1, Volt. swing level 0 2
00102 3C Max Swing Reached = 1 2
00102 3C Training Patt. 2, with Pre-emphasis level 3 2
00102 3C Max Pre-emphasis Reached = 1 2
353 00102 3C TRAINING LANE 2 SET 2 01000 1 Plugged <99,875 us
00102 3C Training Patt. 1, Volt. swing level 0 2
00102 3C Max Swing Reached = 1 2
00102 3C Training Patt. 2, with Pre-emphasis level 3 2
00102 3C Max Pre-emphasis Reached = 1 2
354 00102 3C TRAINING LANE 3 SET 3 01001 1 Plugged <00,125 us
00102 3C Training Patt. 1, Volt. swing level 0 3
Measurements Trigger
For Help, press F1
Tektronix
Start TLA - [Aux Listing] DP Probe Mgr - SN:2906105 3:08 PM

Symbol files

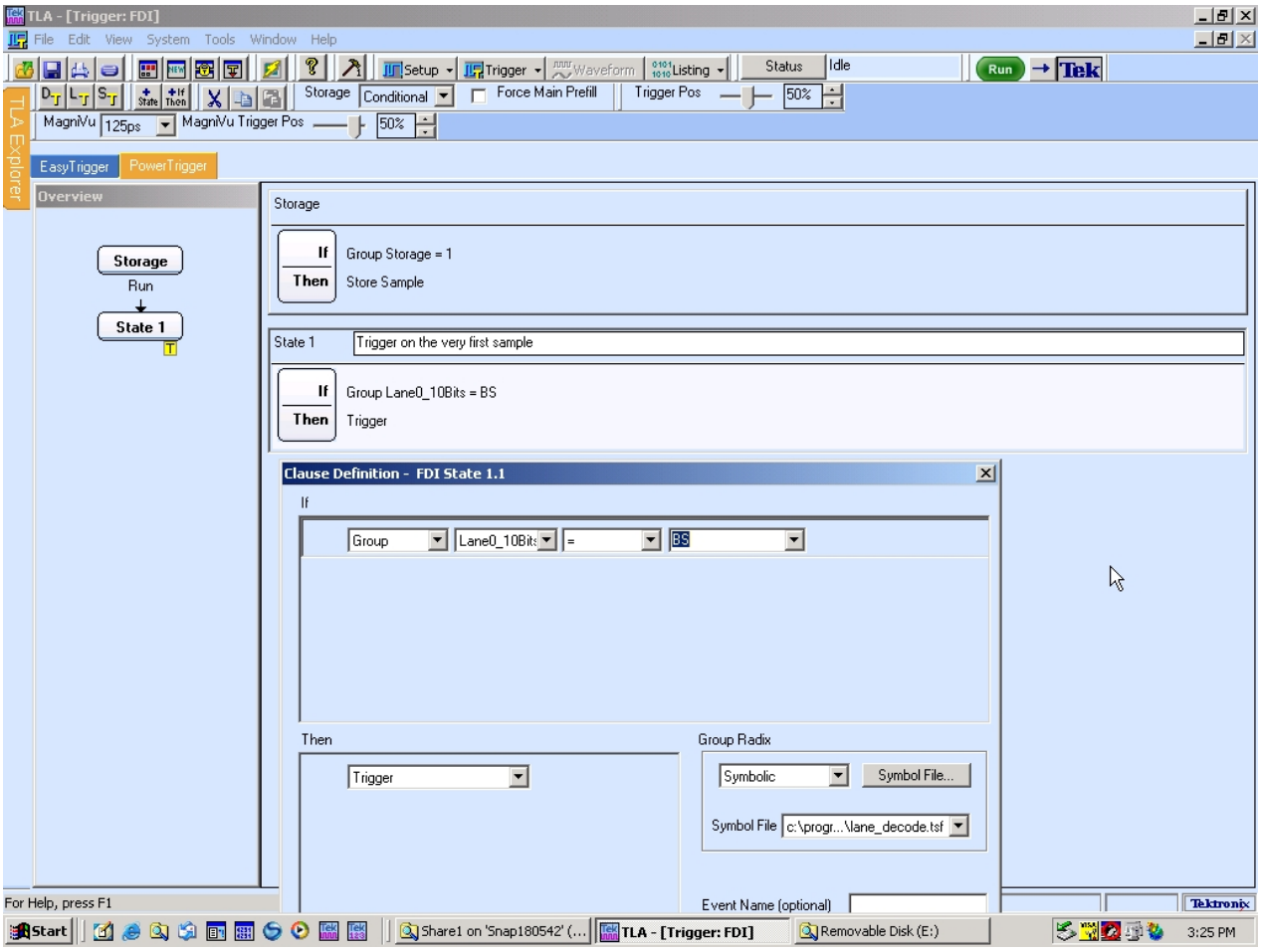
The Support package includes symbol files for the following:

- DP lane data
- Event Codes
- AUX channel Commands
- 10b decode

These are separate files that can be loaded to provide more information in the lister or for use in defining triggers.

Triggering

The system files allow logic analyzer based trigger set-ups that utilize the pre defined symbols described earlier.

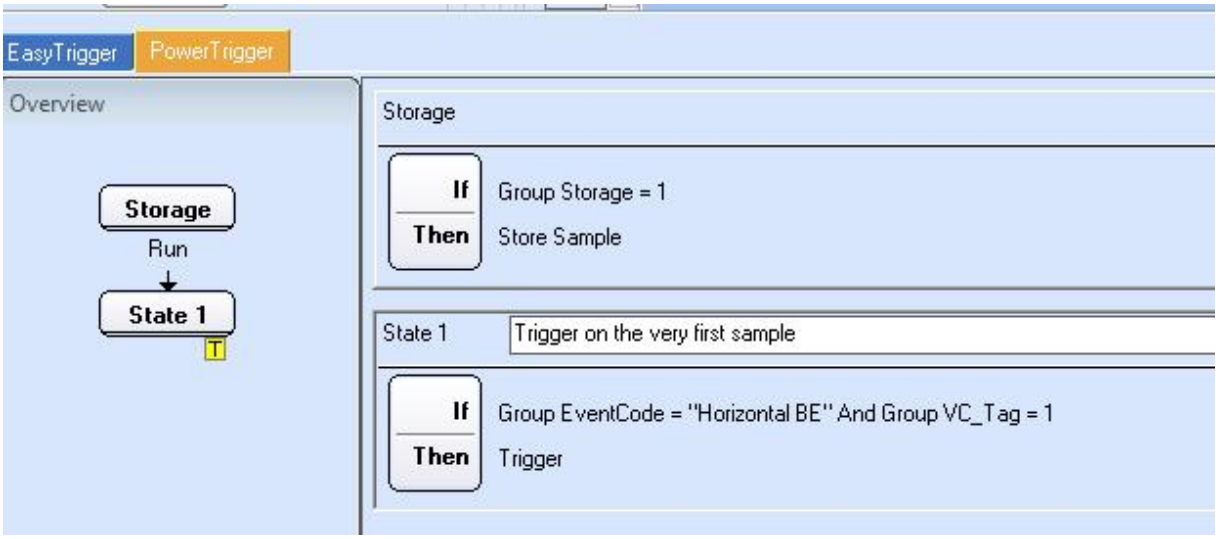


- Remember to always use Conditional Storage. This is because the preprocessor clock is free running and the Storage bit is used to qualify what is sent to the logic analyzer modules. There is a separate storage bit for HPD, HPD_Valid.
- The Event Code field makes it easy to trigger on particular packet types.

To capture specific traffic use the channel signals that can assist in identifying the activity that you want to capture. For example, to capture training use the channel TRAIN, which goes high during training activity. Turning off descrambling when looking at training will properly display the K characters.

Triggering with MST traffic

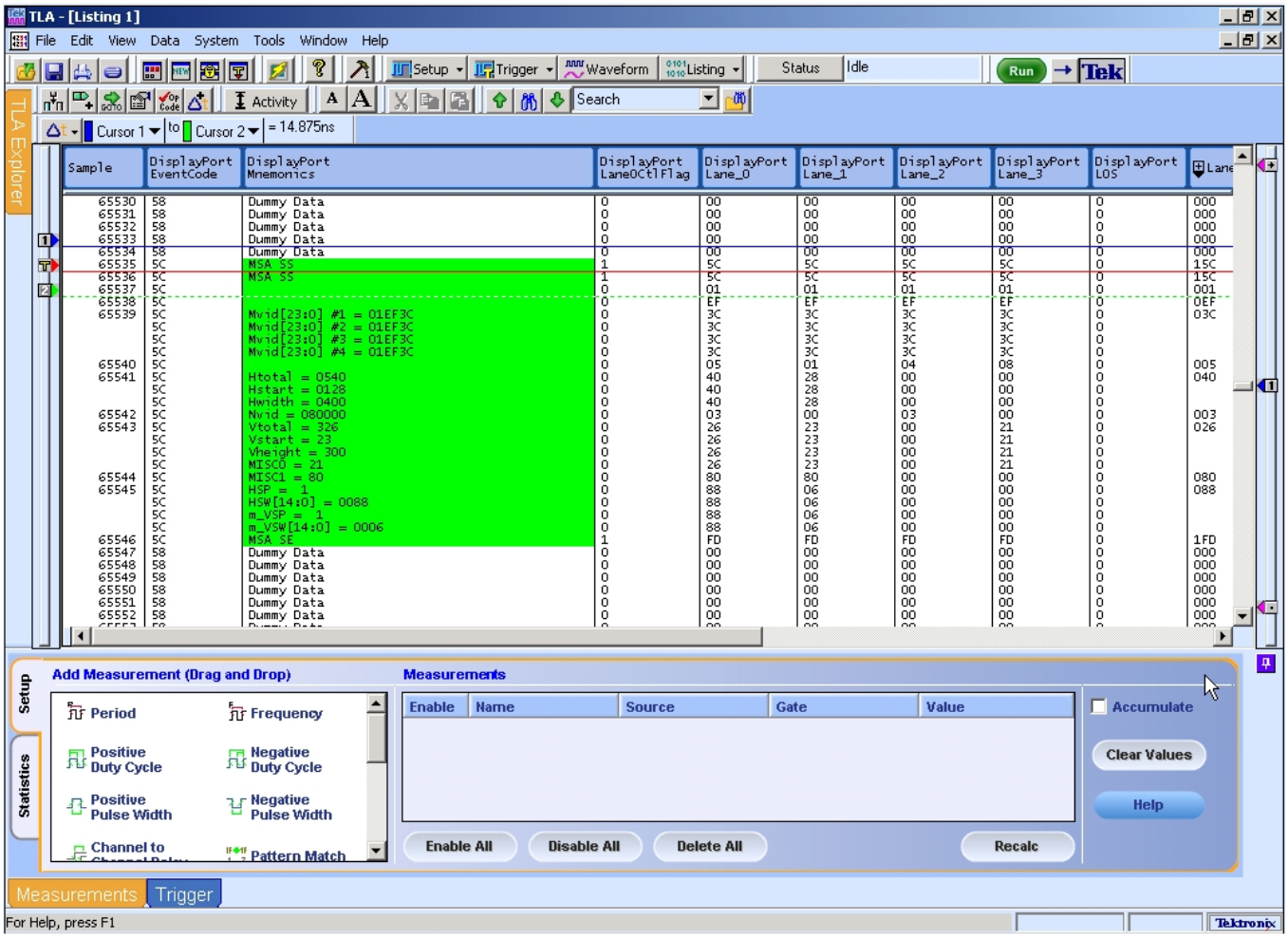
When specifying a trigger with MST traffic it is necessary to add an additional qualifier. The qualifier to use is the group label called VC_Tags and set that value to the value of the virtual channel you want to see. Below is a picture showing an example trigger in MST.



Notice VC_Tag is set equal to 1 for virtual channel 1.

The Protocol Disassembler

Captured DP data is as shown in the following figure. The figure below displays the Main Link protocol decode.



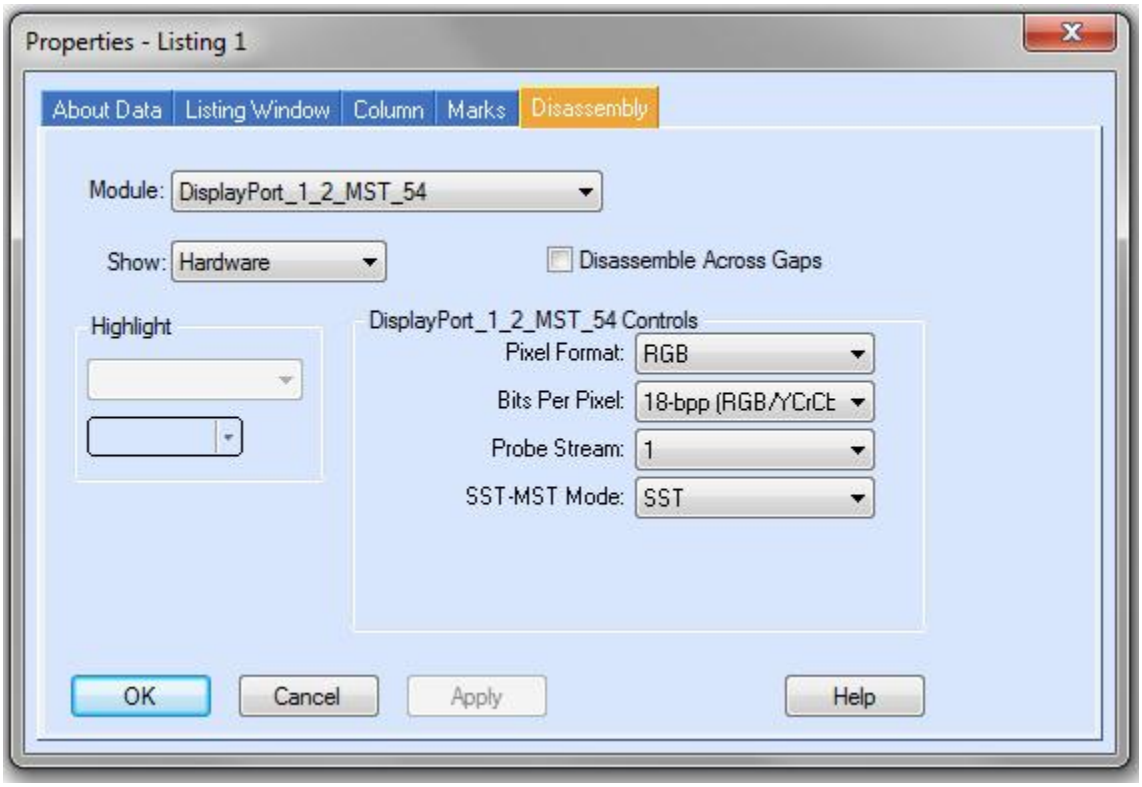
The FS4438 Disassemblers will perform the following functions:

- Decode all DP or AUX, protocol data
- Color code the transaction type. The colors used by the software are as follows:
  - Main Stream Attributes: Green
  - Secondary Data Packets: Blue
  - All other states: White
  - AuxPort: Source initiated: Green

In order for the FS4438 Main Link DP Disassembler to decode the pixel data they must be set to the proper Pixel Width which is found in the Properties tab of it's column heading.

Properties of the Dis-assembler

In order for the dis-assembler to properly decode the captured data the properties need to be set correctly. If you are capturing MST traffic you must set the mode of the dis-assembler for MST mode and select the stream that you want to decode. If running in SST mode select SST mode. In addition to setting the mode, you must set correct pixel format as well as Bits per pixel setting. To access the properties for the dis-assembler, from the listing window right click on the Mnemonics column and select Properties, a window should pop up like the one below, then select the "Disassembly" tab. Once all selections have been made click "OK" to apply the settings, if you have several listing windows open that contain the dis-assembler you must make the selections to each window.



DisplayPort High Speed Groups

Besides de-serializing the data stream for the logic analyzer, the FS4438 generates a number of identification and control bits that are used by the Disassembler and logic analyzer. These are also available to the user and are described below. AUX port is defined separately.

v1.1a mode Logic analyzer signals per pod

Field	Bits	Definition	Pod	Bits
Storage	1	1=store	A4	16
Data Error	1	1=error		15
Train1.1	1	1= DP1.1a training		14
spare	1			13
Probe DP1.1a Mode	**1**	**0= Probe is in DP1.1a mode**		**12**
Pixel Not Recognizer	1	1= Pixel is detected with wrong color		11
Event Code	8	Describes packet type, signal event, or error event		10:3
spare	3			2:0
spare	2		A3	16:15
Data Present [3,2,1,0]	4	1= lane data byte is present		14:11
LOS [3,2,1,0]	4	1= lane loss of signal		10:7
Lane 0 Invalid	1	1= 8b10b error		6
Lane 0 Command	1	1= Control symbol 0 = Data symbol		5
Lane 0 Data [7:3]	5	8b decoded value		4:0
Lane 0 Data [2:0]	3	8b decoded value	A2	16:14
Lane 1 Invalid	1	1= 8b10b error		13
Lane 1 Command	1	1= Control symbol 0 = Data symbol		12
Lane 1 Data [7:0]	8	8b decoded value		11:4
Lane 2 Invalid	1	1= 8b10b error		3
Lane 2 Command	1	1= Control symbol 0 = Data symbol		2
Lane 2 Data [7:6]	2	8b decoded value		1:0
Lane 2 Data [5:0]	6	8b decoded value	A1	15:10
Lane 3 Invalid	1	1= 8b10b error		9
Lane 3 Command	1	1= Control symbol 0 = Data symbol		8
Lane 3 Data [7:0]	8	8b decoded value		7:0

Clock is on A1 bit 16

Event Code symbol definitions mode v1.1a

Event Code Symbol	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
								Err bits	Err bits
		Video	Field						
Mismatch	0	0	x	x	x	x	x	x	1
F0 Pixel	0	1	0	0	0	1	x	0	0
F0 Stuff Data Sym (including FS/FE)	0	1	0	0	1	0	x	0	0
BS	0	1	x	0	1	1	x	0	0
SR	0	1	x	1	0	0	x	0	0
Content Protection BS	0	1	x	1	0	1	x	0	0
BF	0	1	x	1	1	0	x	0	0
F1 Pixel	0	1	1	0	0	1	x	0	0
F1 Stuff Data Sym (including FS/FE)	0	1	1	0	1	0	x	0	0
		Blanking	Horizontal						
Missed SR Hor. Blank BE	0	0	0	0	0	0	1	1	x
Horizontal Blanking BE	0	0	0	0	0	0	1	0	0
Horizontal Blanking VBID	0	0	0	0	0	1	0	0	0
Horizontal Blanking MVID	0	0	0	0	0	1	1	0	0
V_err Hor. Blank MVID	0	0	0	0	0	1	1	1	x
Horizontal Blanking MAUD	0	0	0	0	1	0	0	0	0
A_err Hor. Blank MAUD	0	0	0	0	1	0	0	1	x
SR	0	0	x	0	1	0	1	0	0
Horizontal Blanking Dummy	0	0	0	0	1	1	0	0	0
Horizontal Blanking Audio Stream	0	0	0	1	0	0	0	0	0
Horizontal Blanking Audio TS	0	0	0	1	0	0	1	0	0
Horizontal Blanking Reserved	0	0	0	1	0	1	0	0	0
Horizontal Blanking Extension	0	0	0	1	0	1	1	0	0
Horizontal Blanking Info Frame	0	0	0	1	1	0	0	0	0
		Blanking	Vertical						
Vertical Blanking BE	0	0	1	0	0	0	1	x	x
BE	0	0	X	0	0	0	1	X	x
Missed SR Ver. Blank BE	0	0	1	0	0	0	1	1	x
Vertical Blanking VBID	0	0	1	0	0	1	0	0	0
Vertical Blanking MVID	0	0	1	0	0	1	1	0	0
V_err Vert. Blank MVID	0	0	1	0	0	1	1	1	x
MVID	0	0	X	0	0	1	1	0	0
Vertical Blanking MAUD	0	0	1	0	1	0	0	0	0
MAUD	0	0	X	0	1	0	0	0	0
A_err Ver. Blank MAUD	0	0	1	0	1	0	0	1	x
Vertical Blanking Dummy	0	0	1	0	1	1	0	0	0
Dummy	0	0	X	0	1	1	0	0	0
Vertical Blanking MSA	0	0	1	0	1	1	1	0	0
MSA	0	0	X	0	1	1	1	0	0
Vertical Blanking Audio Stream	0	0	1	1	0	0	0	0	0
Audio Stream	0	0	X	1	0	0	0	0	0
Vertical Blanking Audio TS	0	0	1	1	0	0	1	0	0
Vertical Blanking Reserved	0	0	1	1	0	1	0	0	0
Reserved	0	0	X	1	0	1	0	0	0
Audio TS	0	0	X	1	0	0	1	0	0

Vertical Blanking Extension	0	0	1	1	0	1	1	0	0
Extension	0	0	X	1	0	1	1	0	0
Vertical Blanking Info Frame	0	0	1	1	1	0	0	0	0
Info Frame	0	0	X	1	1	0	0	0	0
Training	1	x	X	X	X	X	X	X	X

v1.2 SST mode Logic analyzer signals per pod

Field	**Bits**	**Definition**	**Pod**	**Bits**
Storage	1	1= store	A4	16
Error bits [2:0]	3	Error bits		15:13
Probe Mode	1	1= Probe is in DP1.2 mode		12
VC Tag [2:0]	3	Virtual Channel tag bits 000 = Probe is in SST Mode		11:9
Pixel Not Recognizer	1	1= Pixel is detected with wrong color		8
Event Code	8	Describes current state or packet type		7:0
not applicable	6	“not applicable” bits are driven low	A3	16:11
LOS [3,2,1,0]	4	1= lane loss of signal		10:7
Lane 0 Invalid	1	1= 8b10b error		6
Lane 0 Command	1	1= Control symbol 0 = Data symbol		5
Lane 0 Data [7:3]	5	8b decoded value		4:0
Lane 0 Data [2:0]	3	8b decoded value	A2	16:14
Lane 1 Invalid	1	1= 8b10b error		13
Lane 1 Command	1	1= Control symbol 0 = Data symbol		12
Lane 1 Data [7:0]	8	8b decoded value		11:4
Lane 2 Invalid	1	1= 8b10b error		3
Lane 2 Command	1	1= Control symbol 0 = Data symbol		2
Lane 2 Data [7:6]	2	8b decoded value		1:0
Lane 2 Data [5:0]	6	8b decoded value	A1	15:10
Lane 3 Invalid	1	1= 8b10b error		9
Lane 3 Command	1	1= Control symbol 0 = Data symbol		8
Lane 3 Data [7:0]	8	8b decoded value		7:0

The Clock is on A1 bit 16

The SST Mode Logic Analyzer bit assignments duplicate the MST Mode bit assignments.

Event Code symbol definitions in SST mode

Event Code Symbol	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F0 Pixel	1	0	0	0	1	0	0	0
F1 Pixel	1	1	0	0	1	0	0	0
BS	0	X	0	0	1	0	1	0
SR	0	x	0	0	1	0	1	1
BE	0	X	0	1	0	1	0	1
F0 Stuff Data Sym (FS/FE)	1	0	0	1	0	0	0	0
F1 Stuff Data Sym (FS/FE)	1	1	0	1	0	0	0	0
Hor. Content. Prot. BS	0	0	1	0	1	0	0	0
Vert. Content. Prot. BS	0	1	1	0	1	0	0	0
Hor. Content. Prot. SR	0	0	1	1	0	0	0	0
Ver. Content. Prot. SR	0	1	1	1	0	0	0	0
Horizontal BS	0	0	0	0	1	0	1	0
Vertical BS	0	1	0	0	1	0	1	0
Horizontal SR	0	0	0	0	1	0	1	1
Vertical SR	0	1	0	0	1	0	1	1
Horizontal BE	0	0	0	1	0	1	0	1
Unknown	0	0	0	0	0	x	0	0
Training TP1	0	0	0	0	0	x	0	1
Training TP2	0	0	0	0	0	X	1	0
Training TP3	0	0	0	0	0	X	1	1
Horizontal VBID	0	0	0	0	1	0	0	1
Vertical VBID	0	1	0	0	1	0	0	1
Horizontal MVID	0	0	0	0	1	1	0	0
Vertical MVID	0	1	0	0	1	1	0	0
Horizontal MAUD	0	0	0	1	0	0	0	1
Vertical MAUD	0	1	0	1	0	0	0	1
Horizontal Dummy	0	0	0	1	1	0	0	1
Vertical Dummy	0	1	0	1	1	1	0	0
Vertical MSA	0	1	0	1	1	1	0	0
Horizontal Audio Stream	0	0	1	0	0	0	0	0
Vertical Audio Stream	0	1	1	0	0	0	0	0
Horizontal Audio TS	0	0	1	0	0	1	0	0
Vertical Audio TS	0	1	1	0	0	1	0	0
Horizontal Audio Copy Mgmt Pkt	0	0	1	0	1	0	1	1
Vertical Audio Copy Mgmt Pkt	0	1	1	0	1	0	1	1
Horizontal ISRC Packet	0	0	1	1	0	0	1	0
Vertical ISRC Packet	0	1	1	1	0	0	1	0
Horizontal VSC Packet	0	0	0	1	0	0	1	0
Vertical VSC Packet	0	1	0	1	0	0	1	0
Horizontal Ext. Packet	0	0	1	1	1	1	0	0
Vertical Ext. Packet	0	1	1	1	1	1	0	0
Horizontal Info. Frame	0	0	0	1	0	1	0	0
Vertical Info. Frame	0	1	0	1	0	1	0	0
Horizontal Reserved	0	0	1	0	0	0	1	1
Vertical Reserved	0	1	1	0	0	0	1	1

Event Code symbol definitions in MST

Event Code Symbol	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F0 Pixel	1	0	0	0	1	0	0	0
F1 Pixel	1	1	0	0	1	0	0	0
BS	0	X	0	0	1	0	1	0
SR	0	x	0	0	1	0	1	1
Horizontal SR	0	0	0	0	1	0	1	1
Vertical SR	0	1	0	0	1	0	1	1
Horizontal BE	0	0	0	1	0	1	0	1
Unknown	0	0	0	0	0	x	0	0
Training TP1	0	0	0	0	0	x	0	1
Training TP2	0	0	0	0	0	X	1	0
Training TP3	0	0	0	0	0	X	1	1
Horizontal VBID	0	0	0	0	1	0	0	1
Vertical VBID	0	1	0	0	1	0	0	1
Horizontal MVID	0	0	0	0	1	1	0	0
Vertical MVID	0	1	0	0	1	1	0	0
Horizontal MAUD	0	0	0	1	0	0	0	1
Vertical MAUD	0	1	0	1	0	0	0	1
Vertical MSA	0	1	0	1	1	1	0	0
Horizontal Audio Stream	0	0	1	0	0	0	0	0
Vertical Audio Stream	0	1	1	0	0	0	0	0
Horizontal Audio TS	0	0	1	0	0	1	0	0
Vertical Audio TS	0	1	1	0	0	1	0	0
Horizontal Audio Copy Mgmt Pkt	0	0	1	0	1	0	1	1
Vertical Audio Copy Mgmt Pkt	0	1	1	0	1	0	1	1
Horizontal ISRC Packet	0	0	1	1	0	0	1	0
Vertical ISRC Packet	0	1	1	1	0	0	1	0
Horizontal VSC Packet	0	0	0	1	0	0	1	0
Vertical VSC Packet	0	1	0	1	0	0	1	0
Horizontal Ext. Packet	0	0	1	1	1	1	0	0
Vertical Ext. Packet	0	1	1	1	1	1	0	0
Horizontal Info. Frame	0	0	0	1	0	1	0	0
Vertical Info. Frame	0	1	0	1	0	1	0	0
Horizontal Reserved	0	0	1	0	0	0	1	1
Vertical Reserved	0	1	1	0	0	0	1	1
SF	X	X	1	1	0	0	1	1
VCPF/RG	X	X	1	1	1	0	0	0
MTP Header = 0	0	0	1	1	1	1	1	1
MTP Header not = SR, 0, or ACT	0	0	1	1	0	1	0	0
MTP Header = ACT	0	0	1	1	0	0	0	1
Unprocessed VC	0	0	0	0	1	1	1	0

SST Mode Event Decode occurs when VC Tag = 0.

The SST Mode Event Decode table otherwise duplicates the MST Mode table.

The Training Type bits are encoded: T[1:0] = 0 indicates symbol error rate measurement pattern. T[1:0] = 1 indicates TP1. T[1:0] = 2 indicates TP2. T[1:0] = 3 indicates TP3. T[2] is a spare.

Error detection

Error Type	**DP1.1a Mode Analyzer Interface**	**SST Mode Analyzer Interface**	**MST Mode Analyzer Interface**
	Data Error	ErrorBit[2:0]	ErrorBit[2:0]
No Error	0	000	000
Mismatch	1	001	001
V_err (MVID Check)	1	010	010
A_err (MAUD check)	1	011	011
Missed SR	1	100	100
Any Invalid	NA	101	101
Loss of Sync	NA	110	110

Mismatch - This error occurs when there when the KChar or configuration fields of the active lanes don't match. Checks are made on all KChars and the VBID, MVID and MAUD fields.

V_err (MVID Check) – This error is detected when the no_video bit is set in the VBID and the MVID field is not 0.

A_err (MAUD check - This error is detected when the audio_mute bit is set in the VBID and the MVAUD field is not 0.

Missed SR

In 1.1a or SST mode - There is a BE counter on each of the four lanes. If 512 BEs are received without receiving an SR on any lane the Missed SR error is asserted.

In MST mode - SR Control Symbol inserted in MTP Header time slot every 1024th MTP as a Link Frame boundary marker, resulting in SR insertion interval of 2^16 time slots. So every 1024th multi-stream transport packet header is replaced with an SR or every 65536 time slot. This SR is for a link frame boundary marker.

Aux Group

Aux Port is a half-duplex, bi-directional channel between DisplayPort transmitter (source) and DisplayPort receiver (sink). It consists of 1 differential pair transporting self-clocked data. The AUX CH supports a bandwidth of **1Mbps.** The DisplayPort Source Device is the master (also referred to as AUX CH requester) that initiates an AUX CH transaction. DisplayPort Sink Device is the slave (also referred to as the replier) is the device that responds to the transaction.

Aux channel has its own clock (67KHz) so that it can be clocked into separate modules in the LA on a separate clock domain. It also has its own Inverse Assembler that has to be loaded separately.

<table>
<tr><th>Field</th><th>Bits</th><th>Definition</th><th>Probe</th><th>Channel</th></tr>
<tr><td>Command</td><td>4</td><td>Command Field</td><td>B1</td><td>3:0</td></tr>
<tr><td>ADDR[11:0]</td><td>12</td><td>Address Field</td><td>B1</td><td>15:4</td></tr>
<tr><td>ADDR[19:12]</td><td>8</td><td>Address Field</td><td>B2</td><td>7:0</td></tr>
<tr><td>Aux CLK</td><td>1</td><td></td><td>B1</td><td>16</td></tr>
<tr><td>DATA[7:0]</td><td>8</td><td>Data field</td><td>B2</td><td>15:8</td></tr>
<tr><td>SYNC</td><td>1</td><td>Sync Bit
First part of the transfer, CMD, ADDR and DATA are all updated, if SYNC is 0 then only DATA is updated.</td><td>B3</td><td>0</td></tr>
<tr><td>STOP
Spare
Spare
Request</td><td>1
1
1
1</td><td>Stop, last byte of the transfer.

High when transaction is request</td><td>B3
B3
B3
B3</td><td>1
2
3
4</td></tr>
<tr><td>Response</td><td>1</td><td>High when transaction is response</td><td>B3</td><td>5</td></tr>
<tr><td>Timeout</td><td>1</td><td>Response Timer timeout period 300us</td><td>B3</td><td>6</td></tr>
<tr><td>HPD event</td><td>2</td><td><table><tr><th>Bit 1</th><th>Bit0</th><th>Meaning</th></tr><tr><td>0</td><td>0</td><td>Unplugged HPD=Low (level)</td></tr><tr><td>0</td><td>1</td><td>HPD pulsed low .25ms to 1.50ms Interrupt event (event signaled on rising edge of HPD)</td></tr><tr><td>1</td><td>1</td><td>Plugged In HPD=High (level)</td></tr></table></td><td>B3</td><td>8:7</td></tr>
<tr><td>HPD Valid</td><td>1</td><td>Indicates a valid HPD event</td><td>B3</td><td>9</td></tr>
<tr><td>Storage</td><td>1</td><td>Indicates Valid states</td><td>B3</td><td>15</td></tr>
<tr><td>Byte Count</td><td>5</td><td>Number of valid bytes received inclusive of current state</td><td>B4</td><td>10:6</td></tr>
</table>

The Storage bit should be used as a qualifier for storing AUX data.

The rate at which Storage is pulsed depends on the packet type. AUX transfers begin with a four bit CMD, a 20 bit address and 8 bits of data. Some packet types contain additional data which will be presented 8 bits at a time. For the additional bytes the Storage bit will be pulsed as each byte is ready, the Command and ADDR Fields will be unchanged.

Acquiring Data

First, insure that the FS4438 is attached to its external power supply and configured, which would be indicated by a green Ready LED. Open up the Probe Manager software and insure the appropriate selections are made and applied, finally make sure that the preprocessor is connected via the appropriate cable(s) to the target system.

Once connected, with the link active, open up the Probe Config window and select cable type, lane width, and reference clock options. Verify that lane activity indicators show activity at the correct lanes. Run the probe and observe the LEDs.

Link Status LED color	Meaning
Green	Lane OK
Dark	Lane not active, or Probe stopped
Orange	Data Invalid (8b10b error)
Red	RX Error (loss of sync or PLL lock)

If a lane's LED is red then there may be a need to select different options for lane width, lane reverse or lane inversion in the Probe Config window.

If a Lane's LED is Orange that indicates some level of Data errors on the link. Check Log file for a count of the errors. BER for a DP link is specified as 10E-9, which at HBR2 (5.4Gbps) allows more than 5 errors every second. All transient events, such as a single bit error or a packet clocked into the analyzer, are stretched to short visible pulses on the LEDs.

We have seen significant sensitivity on HBR2 links to Source settings and the cable used between the Source and Sink.

We recommend the following steps if Lane LEDs are Orange:

1. Use the 2m DP – DP cable provided by FuturePlus with the FS4438.
2. Increase the HS lane signal swing from the DP source.
3. Adjust the Serdes settings in the Probe Configuration form of the Probe Manager.

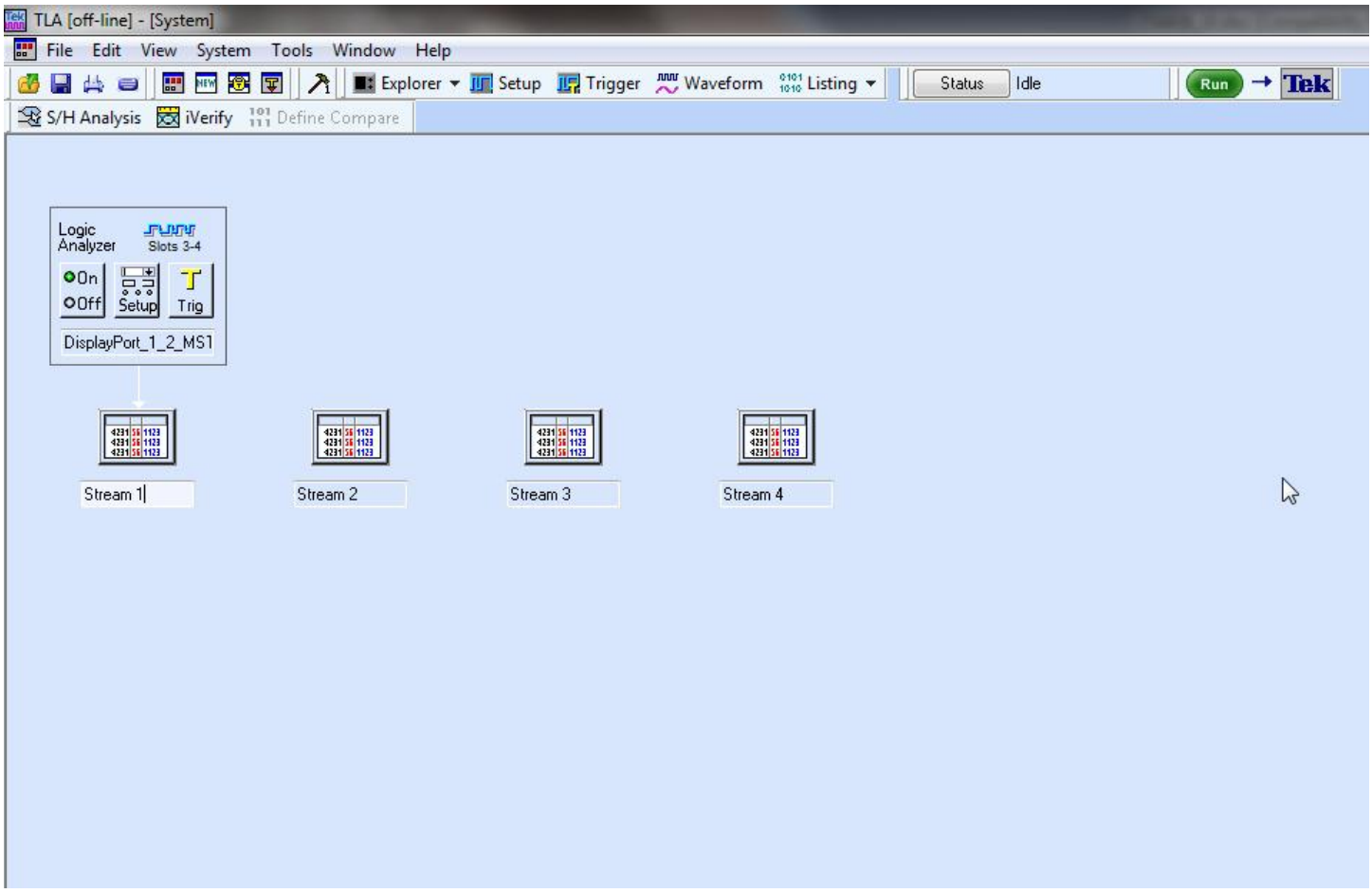
The FS4438 should show a green Signal LED of any Link being probed. Configure the analyzer trigger menu to acquire data. Select RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full; the trigger specification is TRUE or when you select STOP.

The following shows the Logic Analyzer Overview screen for MST operation with 4 Virtual Streams defined. 4 Stream is the maximum # of streams that can defined.

There are 5 State Listings defined:

1. MST Listing – This shows an integrated view of all streams on the HS links. Each state is labeled by it's Stream and has it's own Event and Error codes. This view is not completely time-correlated with the sequence of events on the probed link because of the processing skews associated with the # of Time Slots defined for each stream.

2. Probe Stream Listings (1:4) – These listings display only the information associated with a particular Virtual Stream. Each listing has its own filter applied to show only the associated stream.



General Information

This chapter provides additional reference information including the characteristics and signal connections for the FS4438 probe.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the FS4438 probe.

Standards Supported

If the product is used in a manner not specified by manufacturer, then the protection provided by the equipment may become impaired.

DisplayPort version 1.1a, v1.2

Power Requirements

100-240VAC, 2 amps.

Logic Analyzer Required

Tektronix 1690x frame and 2 of either 40 or 90 pins modules.

Environmental Temperature

Operating: 20 to 30 degrees C (68 – 86 degrees F)

Altitude

Operating: 4,6000m (15,000 ft)

Non operating: 15,3000m (50,000 ft)

Humidity

Up to 80% relative humidity. Avoid sudden, extreme temperature changes which would cause condensation on the FS4438 module.

Testing and Troubleshooting

There are no automatic performance tests or adjustments for the FS4438 module. If a failure is suspected in the FS4438 module contact the factory or your FuturePlus Systems authorized distributor.

Servicing

The repair strategy for the FS4438 is module replacement. However, if parts of the FS4438 module are damaged or lost contact the factory for a list of replacement parts.